Notes on BJT & FET Transistors.

Comments.

The name *transistor* comes from the phrase "*trans*ferring an electrical signal across a res*istor*."

In this course we will discuss two types of transistors:

The **Bipolar Junction Transistor (BJT)** is an active device. In simple terms, it is a *current controlled* valve. The *base current* (I_B) controls the *collector current* (I_C).

The **Field Effect Transistor (FET)** is an active device. In simple terms, it is a *voltage controlled* valve. The *gate-source voltage* (V_{GS}) controls the *drain current* (I_D).

Regions of BJT operation:

Cut-off region: The transistor is off. There is no conduction between the collector and the emitter. ($I_B = 0$ therefore $I_C = 0$)

Active region: The transistor is on. The collector current is proportional to and controlled by the base current ($I_C = \beta I_C$) and relatively insensitive to V_{CE}. In this region the transistor can be an amplifier.

Saturation region: The transistor is on. The collector current varies very little with a change in the base current in the saturation region. The V_{CE} is small, a few tenths of volt. The collector current is strongly dependent on V_{CE} unlike in the active region. It is desirable to operate transistor switches will be in or near the saturation region when in their *on* state.

Rules for Bipolar Junction Transistors (BJTs):

- For an *npn* transistor, the voltage at the collector V_C must be greater than the voltage at the emitter V_E by at least a few tenths of a volt; otherwise, current will not flow through the collector-emitter junction, no matter what the applied voltage at the base. For *pnp* transistors, the emitter voltage must be greater than the collector voltage by a similar amount.
- For the *npn* transistor, there is a voltage drop from the base to the emitter of 0.6 V. For a *pnp* transistor, there is also a 0.6 V rise from the base to the emitter. In terms of operation, this means that the base voltage *V*B of an *npn* transistor must be at least 0.6 V greater that the emitter voltage *V*E; otherwise, the transistor will pass an emitter-to-collector current. For a *pnp* transistor, *V*B must be at least 0.6 V less than *V*E; otherwise, it will not pass a collector-to-emitter current.

BASIC EQUATIONS FOR THE BJT.

for npn : $V_B > V_E + 0.6\,\text{V}$

for pnp : $V_B < V_E - 0.6\,\text{V}$

for both npn & pnp anytime

$$I_E = I_C + I_B$$

for both npn & pnp only in the active region

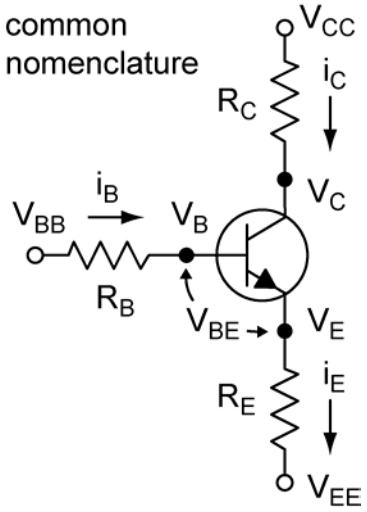
$$I_C = h_{FE} I_B = \beta I_B$$

$$I_E = I_C + I_B = (\beta + 1) I_B \approx \beta I_B$$

BJT Schematic Symbols (Mnemonics for remembering the direction of the arrows are in parenthesis.)

Ohmmeters view of the BJT. Clearly a transistor cannot be made on the bench by combining two resistors. (Why is that?) Most ohmmeters can not only measure the resistance, but also measure the forward voltage drop across a diode. From this perspective you can identify the base and the type of transistor based on the following equivalent circuits.

Common Nomenclature (*npn* example).



Types of Amplifiers.

The transistor is a three terminal device, thus the input and the output must share one terminal in *common.* This is the origin of the nomenclature of the three types of transistor amplifiers: common collector, common emitter, and common base.

Definition of Gain.

Gain is defined as the ratio of the output signal to the input signal. Because transistor amplifiers often have a quiescent output (a non zero output when the input is zero) we define gain as the derivative of the output with respect to the input. For systems where the quiescent output is zero, this reduces to the ratio of the output to the input. Thus gain is defined as the ratio of the change in output to the change in input.

So far we have not specified the output quantity, the reason is that we can define the gain with respect to any given output and input quantity.

General definition : $A = \frac{\mathrm{d}(Output)}{\mathrm{d}(Input)}$ if $(Output) = 0$ when $(Input) = 0$, then $A = \frac{(Output)}{(Input)}$

Voltage Gain : $A_V = \frac{\mathrm{d}V_{out}}{dV_{in}}$ if $V_{out} = 0$ when $V_{in} = 0$, then $A = \frac{V_{out}}{V_{in}}$

Current Gain : $A_I = \frac{\mathrm{d}I_{out}}{dI_{in}}$ if $I_{out} = 0$ when $I_{in} = 0$, then $A = \frac{I_{out}}{I_{in}}$

Power Gain : $A_P = \frac{\mathrm{d}P_{out}}{dP_{in}}$ if $P_{out} = 0$ when $P_{in} = 0$, then $A = \frac{P_{out}}{P_{in}}$

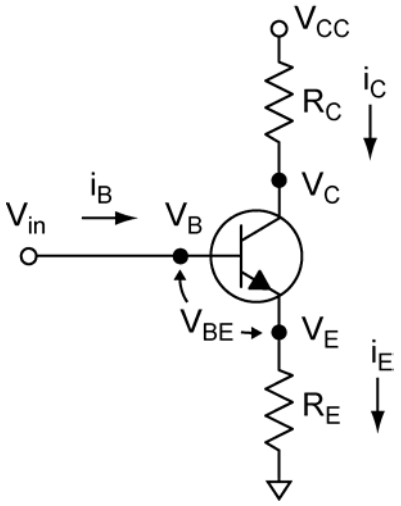
Note that a negative gain means that the sign of the signal is inverted. Negative gain is not possible for Power Gain. |A| less than unity indicates that the output is smaller than the input.

The quantities need not be the same. If the input and output quantities are different, the gain is no longer unitless. The most common examples are transimpedance gain and transadmittance gain.

Transmpedance Gain : $A_Z = \frac{\mathrm{d}V_{out}}{dI_{in}}$ if $V_{out} = 0$ when $I_{in} = 0$, then $A = \frac{V_{out}}{I_{in}}$

Transadmittance Gain : $A_Y = \frac{\mathrm{d}I_{out}}{dV_{in}}$ if $I_{out} = 0$ when $V_{in} = 0$, then $A = \frac{I_{out}}{V_{in}}$

Input Impedance of a Transistor.



Impedance is defined as $Z = V/I$. In linear circuits (with resistors, capacitors, inductors, batteries, etc.) this ratio is the reciprocal of the slope of the I versus V graph. In circuits with nonlinear elements such as a transistor, the input impedance of the transistor is defined as the reciprocal of the slope of the I versus V graph. This is simply the derivative of V_{in} with respect to I_{in}.

$$Z_{in} = \frac{\mathrm{d}V_{in}}{\mathrm{d}I_{in}}$$

We can easily find Z_{in} from what we know already of the behavior of the transistor. We know that the sum of V_{BE} and the IR drop across R_{E} must equal V_{in}.

$$V_{in} = V_B = V_{BE} + V_E = V_{BE} + I_E R_E \qquad I_E = I_C + I_B = \beta I_B + I_B = I_B(\beta + 1)$$

$$V_{in} = V_{BE} + I_E R_E = V_{BE} + I_B(\beta + 1)R_E \qquad I_B = I_{in}$$

$$V_{in} = V_{BE} + I_{in}(\beta + 1)R_E$$

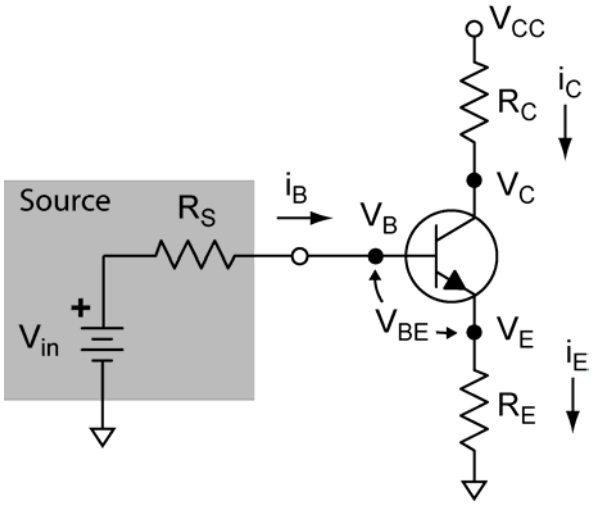
Taking the derivative of V_{in} with respect to I_{in}, remembering that V_{BE} is a constant, we get the result:

$$Z_{in} = \frac{\mathrm{d}V_{in}}{\mathrm{d}I_{in}} = \frac{\mathrm{d}}{\mathrm{d}I_{in}}\left(V_{BE} + I_{in}(\beta + 1)R_E\right) = (\beta + 1)R_E$$

$$\boxed{Z_{in} = (\beta + 1)R_E \approx \beta R_E}$$

Because $I_{\text{E}} = I_{\text{B}}(\beta + 1)$ The IR drop across R_{E} is greater than it would be for I_{B} alone. The amplification of the base current causes R_{E} to appear larger to a source looking into the input by $(\beta + 1)$.

Output Impedance of a Transistor for the Emitter Follower (Common Collector).



The output impedance seen by the load (R_E in this example) is defined as:

$$Z_{out} = -\frac{\mathrm{d}V_{out}}{\mathrm{d}I_{out}}$$

The minus sign in the derivative comes from the fact the output impedance has the effect of decreasing V_{out}. The output current I_{out} is just the emitter current I_E which is related to the base current.

$$V_{in} = I_B R_S + V_{BE} + V_E \qquad V_{out} = V_E$$

$$V_{out} = V_E = V_{in} - I_B R_S - V_{BE} \qquad I_{out} = I_E \qquad I_B = \frac{I_E}{\beta + 1}$$

$$V_{out} = V_{in} - \left(\frac{I_E}{\beta+1}\right)R_S - V_{BE} = V_{in} - \left(\frac{I_{out}}{\beta+1}\right)R_S - V_{BE} = -I_{out}\left(\frac{R_S}{\beta+1}\right) + \left(V_{in} - V_{BE}\right)$$

$$Z_{out} = -\frac{\mathrm{d}V_{out}}{\mathrm{d}I_{out}} = -\frac{\mathrm{d}}{\mathrm{d}I_{out}}\left(-I_{out}\left(\frac{R_S}{\beta+1}\right) + \left(V_{in} - V_{BE}\right)\right) = \left(\frac{R_S}{\beta+1}\right)$$

Thus we obtain the result that the impedance of the source, as viewed by the load, is reduced by the factor ~1/β.

$$\boxed{Z_{out} = \left(\frac{R_S}{\beta+1}\right) \approx \frac{R_S}{\beta}}$$

The Field Effect Transistor (FET).

FETs is a three terminal device like the BJT, but operates by a different principle. The three terminals are called the source, drain, and gate. The voltage applied to the gate controls the current flowing in the source-drain channel. No current flows through the gate electrode, thus the gate is essentially insulated from the source-drain channel. Because no current flows through the gate, the input impedance of the FET is extremely large (in the range of 10^{10}–10^{15} Ω). The large input impedance of the FET makes them an excellent choice for amplifier inputs.

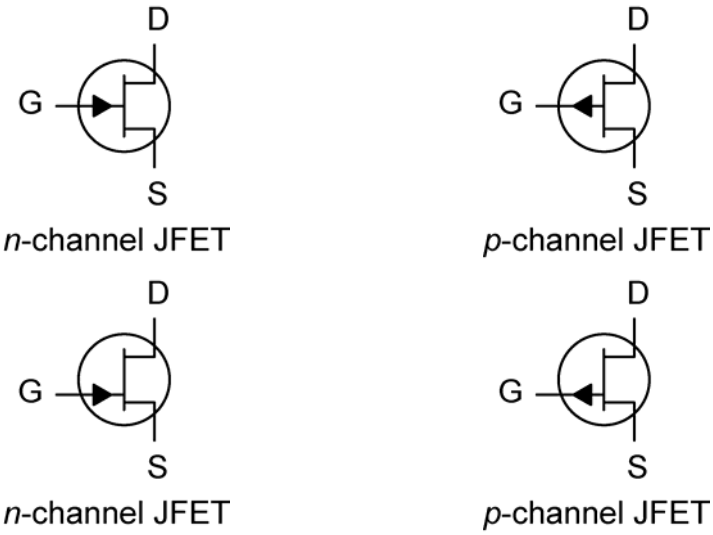
The two common families of FETs, the junction FET (JFET) and the metal oxide semiconductor FET (MOSFET) differ in the way the gate contact is made on the source-drain channel.

In the JFET the gate-channel contact is a reverse biased *pn* junction. The gate-channel junction of the JFET must always be reverse biased otherwise it may behave as a diode. All JFETs are depletion mode devices—they are *on* when the gate bias is zero ($V_{GS} = 0$).

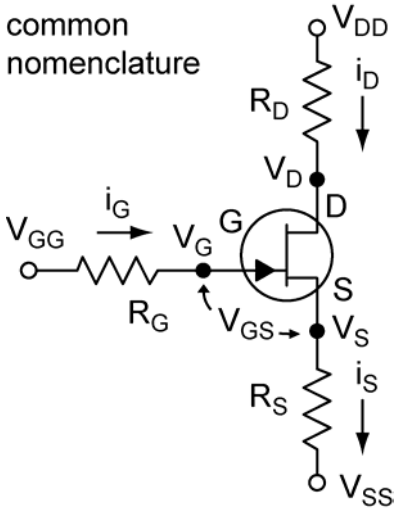
In the MOSFET the gate-channel contact is a metal electrode separated from the channel by a thin layer of insulating oxide. MOSFETs have very good isolation between the gate and the channel, but the thin oxide is easily damaged (punctured!) by static discharge through careless handling. MOSFETs are made in both depletion mode (*on* with zero biased gate, $V_{GS} = 0$) and in enhancement mode (*off* with zero biased gate).

In this class we will focus on JFETs.

Schematic symbols. Two versions of the symbols are in common use. The symbols in the top row depict the source and drain as being symmetric. This is not generally true. Slight asymmetries are built into the channel during manufacturing which optimize the performance of the FET. Thus it is necessary to distinguish the source from the drain. In this class we will use the asymmetric symbols found on the bottom row, which depict the gate nearly opposite the source. The designation *n*-channel means that the channel is *n* doped and the gate is *p* doped. The *p*-channel is complement of *n*-channel.



Common Nomenclature (*n*-channel FET example).



Regions of JFET operation:

Cut-off region: The transistor is off. There is no conduction between the drain and the source when the gate-source voltage is greater than the cut-off voltage. ($I_D = 0$ for $V_{GS} > V_{GS,off}$)

Active region (also called the Saturation region): The transistor is on. The drain current is controlled by the gate-source voltage (V_{GS}) and relatively insensitive to V_{DS}. In this region the transistor can be an amplifier.

In the active region: $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS,off}}\right)^2$$

Ohmic region: The transistor is on, but behaves as a voltage controlled resistor. When V_{DS} is less than in the active region, the drain current is roughly proportional to the source-drain voltage and is controlled by the gate voltage.

In the ohmic region:

$$I_D = I_{DSS}\left[2\left(1 - \frac{V_{GS}}{V_{GS,off}}\right)\frac{V_{DS}}{-V_{GS,off}} - \left(\frac{V_{DS}}{V_{GS,off}}\right)^2\right]$$

$$R_{DS} \approx \frac{V_{GS,off}}{2I_{DSS}\left(V_{GS} - V_{GS,off}\right)} = \frac{1}{g_m}$$

Common Specifications.

$\boldsymbol{I_{DSS}}$ is the drain current in the active region for $V_{GS} = 0$. (I_D source shorted to gate)

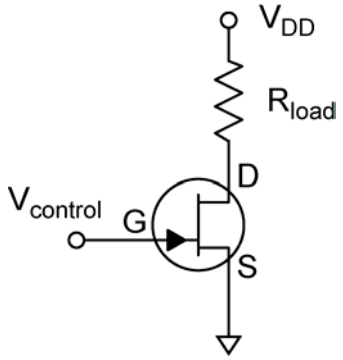
$\boldsymbol{V_{GS,off}}$ is the minimum V_{GS} where $I_D = 0$. $V_{GS,off}$ is negative for *n*-channel and positive for *p*-channel..

$\boldsymbol{g_m}$ is the transconductance, the change in I_D with V_{GS} and constant V_{DS}.

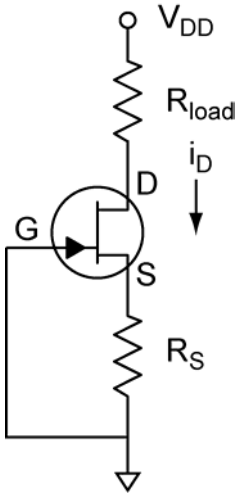
$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}} = \frac{2I_{DSS}}{V_{GS,off}}\left(V_{GS} - V_{GS,off}\right)$$

Common Circuit Applications:

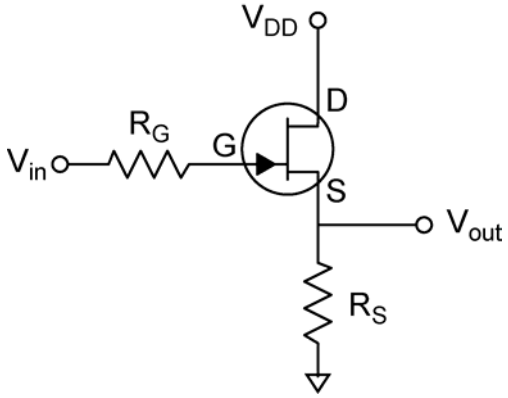
Voltage Controlled Switch. For the *on* state the gate voltage $V_{GS} = 0$ and for the *off* state $|V_{GS}| > |V_{GS,off}|$ (of great magnitude than $V_{GS,off}$ and with the same sign). The sign of the voltage depends on the type of FET, negative for *n*-channel and positive for *p*-channel.

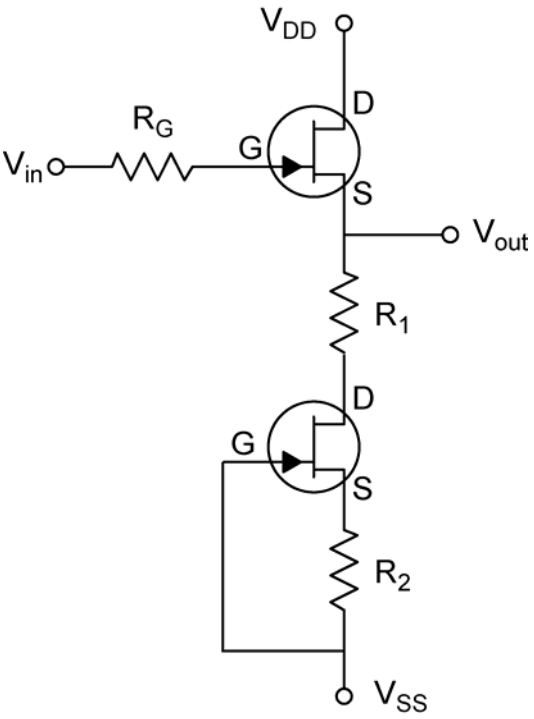


Current Source. The drain current is set by R_S such that $V_{GS} = I_D R_S$. Any value of current can be chosen between zero and I_{DSS} (see the I_D vs V_{GS} graph for the JFET).

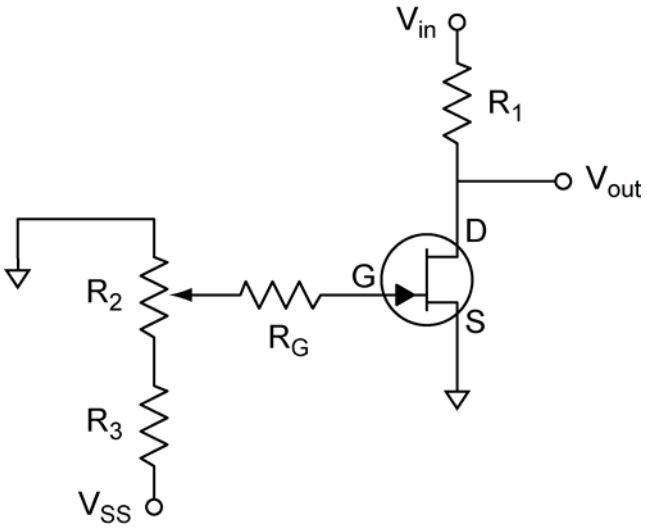


Source Follower. The simple source follower is shown below. The improved version is shown at the right. The lower JFET forms a current source. The result is that V_{GS} is held constant, removing the defects of the simple circuit.





Voltage-Controlled Resistor. V_{GS} must be between zero and $V_{GS,off}$.



JFET Diode. The JET *pn* gate junction can be used as a diode by connecting the source and the drain terminals. This is done if very low reverse leakage currents are required. The leakage current is very low because the reverse leakage current scales with the gate area. Small gate areas are designed into JFETs because it decreases the gate-source and the gate-drain capacitances