Lab #15: Introduction to Computer Aided Design

Revision: 02 Nov 2016

Print Name:	Section:

GETTING FAMILIAR WITH YOUR BASYS3 DIGILAB BOARD.

Problem 1: (26 points) Visually inspect the Digilab board, enter the number of components in the blanks for all entries. (Get to know the board.)

COUNT ONLY INSTALLED DEVICES! Some positions are empty.

count	item
	resistors (Rx)
	capacitors (Cx)
	LEDs (LDx)
	7-segment display digits
	pushbutton switches
	slide switches
	diodes (Dx)

count	item
	integrated circuits (ICx)
	connectors (e.g J8 & JD)
	jumpers (e.g. JP4 & J7)
	inductors (Lx)
	crystal oscillator (X1)
	transistors (Qx)

Problem 2: (16 points) Complete the following test procedure for the Digilab board, circling Y (for Yes) or N (for No) for all entries.

Manual Test Procedure

Section 1. Power-on test. Connect USB cable to the board and to your computer. Locate JP2, set shunt to USB position (power from USB).

1.1	Proper USB cable obtained	Y	N
1.2	Power-on LED illuminates brightly	Y	N

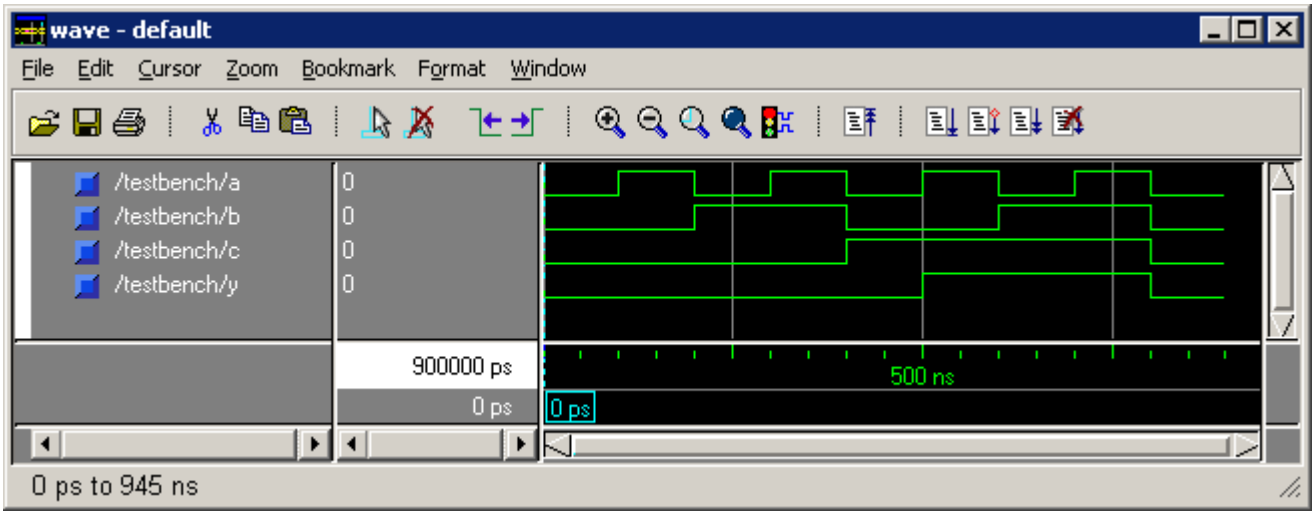
Section 2. Manual tests

2.1	red “power” LED illuminates when power switch is in the on position	Y	N
2.2	When program button pressed, green “done” LED goes out and amber ‘busy” LED comes on. When button is released, the LEDs return to their initial states after a brief delay.	Y	N

Section 3. Automated tests (diagnostic program running at initial power up).

3.1	The 4 display digits count 0 – 9 with no dark segments	Y	N
3.2	All buttons function correctly (BTNx)	Y	N
3.3	All switches function correctly (sw0-sw15)	Y	N
3.4	LEDs function correctly (led0-led15)	Y	N

Problem 3: (8 points) Create a truth table from simulation data. The following simulation shows the logic states of the 3 inputs and of the output as functions of time. The green trace shows the states of each signal at different points in time. Naturally there are only two states for each. When the green trace is low, the state is 0 (zero), when it is high, the state is 1. Thus the far left end of the trace shows a=0, b=0, c=0, and y=0. Proceeding to the right, we see that a changes state so that we then have a=1, b=0, c=0, and y=0. Continuing to the right, the next change gives us a=0, b=1, c=0, and y=0. The entire truth table can be read off such a representation of the states of the system provided that enough combinations are displayed. The time dependence is not important here, but it gives us a simple way to see the output voltage at all possible combinations of the input voltages.



Create a truth table that corresponds to the simulation shown above. Show all input and output values in the truth table, and sketch a logic circuit that could have been used to create the waveform.

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Problem 4: (15 points) Use the Vivado Design Suite to create separate VHDL code blocks for each of the following logic statements. Be sure to assign both inputs and outputs so they match the ports defined in the constraints file (XDC file). Also connect A, B, and C to outputs so you can more easily troubleshoot your circuit. For testing, assign the inputs A, B, & C to sw0, sw1, & sw2, respectively. Assign the outputs A, B, & C to led0, led1, & led2, respectively, and the remaining output to led3. When the circuits have been completed and simulated, print, and attach a copy of each VHDL code block & XDC file to your lab report.

1) Y = A'C + AB'C' 2) F = BC' + A'BC + A'C' 3) G = (A+B+C)(A'+C')(B'+C')

Problem 5: (15 points) Adapt the three VHDL code blocks from problems 4a, 4b, and 4c as lower level modules and use them in a new top-level VHDL code block. Include three inputs (A, B, C; sw0-sw2) and six outputs (A, B, C, Y, F, G; led0-led5), and Use the same A, B, and C signals as inputs for the instances of each lower level module. Program the Basys3 board to verify you have a working implementation. Demo this circuit to the lab assistant and have them initial your lab submission form. Attach printed a copies of the top-level VHDL code block, the lower level modules, and the XDC file.

demo date:

TA initials:

Problem 6: (20 points) Implement a circuit for the Overhead Coffee Company buy decision. Show any work performed in arriving at a minimal circuit below. Implement the circuit in VHDL using the Vivado Design Suite, and then program the logic on the Digilab board. Demo this circuit to the lab assistant and have them initial your lab submission form. Attach a printed a copy of the VHDL code block, the lower level modules (if any), and the XDC file.

demo date:

TA initials:

Homework (100 points)

1. (16 points) Sketch circuits for the following logic equations. Recall a tick mark (‘) following a variable or parenthetical expression means to invert that variable or expression.

   Y = BC + A’D

   F= (A’B) XOR (C + D)’

   G = ((AB’)’ + BC’)’

   Z = ((A + C)·(B+D)’)’

2. (18 points) Sketch minimal circuits defined by the truth tables below.

A	B	C	F
L	L	L	1
L	L	H	1
L	H	L	0
L	H	H	0
H	L	L	0
H	L	H	0
H	H	L	1
H	H	H	1

A	B	C	F
L	L	L	0
L	L	H	1
L	H	L	0
L	H	H	0
H	L	L	1
H	L	H	1
H	H	L	0
H	H	H	0

A	B	C	F
L	L	L	1
L	L	H	0
L	H	L	1
L	H	H	0
H	L	L	1
H	L	H	0
H	H	L	1
H	H	H	0

3. (20 points) Simplify the following expressions using the laws of Boolean Algebra

A. A(B’ + A’) + C’(A + B’)

B. (X + Y’)(X’Z + Y’)

C. (A + AB’ + (B’C)’)’

D. A’B + A’B’C + AD’ +ACD’

E. (AB)C’ + (AB)’C

5. (18 points) In a logic function with n inputs, there are 2^n unique combinations of inputs and 2^{2^n} possible logic functions. The table below has four rows that show the four possible combinations of two inputs ($2^2 = 4$), and 16 output columns that show all possible two-input logic functions ($2^{2^2} = 16$). Some of these output columns are associated with logic circuits, and some are not. Write the name of the logic function in the blanks below the output columns, or write N/A if the column is not associated with a common function (4 blanks have already been filled in).

2^n Inputs		ALL 2^{2^n} POSSIBLE LOGIC FUNCTION OUTPUTS															
A	B	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
LV	LV	LV	HV	LV	HV	LV	HV	LV	HV	LV	HV	LV	HV	LV	HV	LV	HV
LV	HV	LV	LV	HV	HV	LV	LV	HV	HV	LV	LV	HV	HV	LV	LV	HV	HV
HV	LV	LV	LV	LV	LV	HV	HV	HV	HV	LV	LV	LV	LV	HV	HV	HV	HV
HV	HV	LV	LV	LV	LV	LV	LV	LV	LV	HV	HV	HV	HV	HV	HV	HV	HV
Function		GND		N/A				XOR									VDD

A table like the one above for 3 inputs would need _____ rows and _____ columns.

A table like the one above for 4 inputs would need _____ rows and _____ columns.

A table like the one above for 5 inputs would need _____ rows and _____ columns.

6. (12 points) In the table below, the voltage levels from the table above have been mapped to 1's and 0's. Six of the columns represent common logic functions of two variables. Circle the six columns, and label them with the circuit function. Draw the circuit symbols for the functions represented.

INPUTS		ALL POSSIBLE OUTPUTS															
A	B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

7. (16 points) Design and sketch a *minimal* four-input circuit that outputs a LHV whenever two or more inputs are asserted.