ATLAS Pixel Detector
Request for Quotation
and
Flexible Circuit Board Manufacturing
Acceptance Criteria

version 1.1

Preamble

This document lists the specifications, acceptance criteria and purchasing instructions for the ATLAS Pixel Detector Flexible Circuit Boards, hereafter referred to as the "flex circuits". In the following, "Vendor" refers to the respondent to this Request for Quotation (RFQ) and "Buyer" refers to the University of Oklahoma.

1 Quantity and Pricing

1.1 Quantity

1.1.1 Even at this late date, the ATLAS Pixel Detector Flex Hybrids are still in development in that certain aspects of their makeup are still being qualified. Because of this, the order will be made in two parts:

1.1.1.1 Part 1: 1000 Good flex circuits

1.1.1.2 Part 2: 2500 Good flex circuits

1.1.2 Good flex circuits are those that have passed all tests and inspections according to the criteria in this document

1.1.3 Part one delivery is required within 8 weeks after receipt of the purchase order. The purchase order will be sent out as soon as possible after bids are opened and a vendor is selected.

1.1.4 Part 2 will be ordered no later than December 24th, 2003. Delivery shall be completed no later than March 15th, 2004.

1.1.5 In addition, we require that those flex circuits that do not qualify as Good flex circuits be delivered. These will be used for tests and processing tuning at OU and other ATLAS Pixel Detector assembly sites. The build up (Section 3) of these defective flex circuits is not required to be complete.

1.2 Prices quoted shall be in the currency of the country to which address payments would be sent. Quoted prices shall be evaluated based on the

exchange rate between the currency in which the quotation is made and US dollars plus import duties, at the time of the bid opening.

2 Required performance is "High Reliability".

The flex circuits will be required to operate for up to ten years without maintenance in a dry nitrogen, zero degree environment. Some temperature cycling to room temperature will occur. See IPC-6011.

3 Construction (Build Up)

3.1 The flexible circuits boards shall be of a single, 2 mil substrate with double metal construction.

3.2 The two metal layers are connected by plated, through hole vias.

3.3 A cover layer or solder resist layer is required over the top metal.

3.3.1 The minimum thickness over any conductor is 7 μm.

3.3.2 Top cover layer placement accuracy shall be ± 127 μm from nominal position, as given in the Gerber files.

3.3.3 Pits and voids are allowed provided they do not expose any portion of any conductor.

3.3.4 Vias which are not covered or are insufficiently covered by solder resist are acceptable, provided the number of affected via holes ≤ 5% of the total number of via holes.

3.3.5 Minimum solder mask width between lands is ≥ 150 μm. Therefor, solder resist breakout shall not be accepted.

3.4 A cover layer or solder resist is required on the bottom layer.

3.4.1 Maximum thickness of the bottom cover layer/solder resist is 127 μm (5 mil).

3.4.2 The bottom cover layer/solder resist shall be capable of holding off up to 1000 Vdc from the flex circuitry beneath it (bottom metal).

3.4.3 No voids, pin holes, scratches or other defects in the bottom cover layer/solder resist which would prevent compliance with the above voltage hold off specification shall be accepted.

3.4.4 No touch-up of bottom cover layer/solder resist voids or holes is allowed.

3.4.5 Bottom cover layer/solder resist placement accuracy shall be ± 127 μm from nominal position, as given in the Gerber files.

3.5 The following table lists the accepted materials for flex circuit construction:

Flexible substrate	50.8 micron polyimide with adhesiveless copper. Acceptable products are: • Espanex ED, 2 mil thick • Upilex-50S, 2 mil thick
Cu profile	16 μm - 25 μm thick, compatible with aluminum ultrasonic wire bonding and reflow soldering
Ni plating	electroless, 2.0 μm thick, ± 20% compatible with aluminum ultrasonic wire bonding and reflow soldering
Au plating	electroless. 0.1 μm - 0.2 μm thick suitable for aluminum ultrasonic wire bonding and reflow soldering
Solder Mask	Acceptable materials: • Pyralux PC1015 • Multiline Intl. Europa L.P. WPS-80 • Espanex + Pyralux LF adhesive

3.6 Markings

3.6.1 There are no silk screen or other ink printed layers in the design.

3.6.2 No markings of any type are acceptable for flex which pass all inspections and tests. Scrap flex circuits (rejected parts) should be marked as such, but the mark(s) shall not cover any bond pads (scrap parts are used for wire bonding tests and calibration).

4 Fabrication Tolerances and Acceptance Criteria

4.1 Dimensions and tolerances of metal pattern (as a whole), holes and substrate dimensions and their tolerances with respect to one another are provided in drawings within the Flex Hybrid Fabrication document (apfh5xfab.pdf).

4.2 Singulation

4.2.1 The individual circuits shall be cut from the panels by laser, knife or steel die.

4.2.2 No burrs, nicks or other defects shall extend more than 0.5 mil from the nominal cut edge of the flex circuit.

4.3 Minimum conductor width

4.3.1 The minimum conductor width shall be $\geq$ 80 % of nominal width, as defined in the flex circuit Gerber files, measured where the conductor trace attaches to the substrate.

4.3.2 An additional reduction of the nominal conductor width, as defined in the flex circuit Gerber files, due to nicks, edge roughness or other localized defects is acceptable, provided the length of any single defect is no more than 1 mm.

4.4 Minimum conductor spacing

4.4.1 The minimum conductor spacing shall be ≥ 80 % of nominal spacing, as defined in the flex circuit Gerber files, measured where the conductor traces attach to the substrate.

4.4.2 A further localized reduction of ≤ 20% in the conductor spacing due to edge roughness, burrs, etc. is allowed provided the local defect is no longer than 1 mm.

4.4.3 Metal orphans between conductors are not acceptable.

4.5 Surface mount lands

4.5.1 Defects such as nicks, scratches and cracks are acceptable as long as they do not exceed the shorter of either the width or length of the land by more than 20%.

4.5.2 The maximum area of an internal defect, such as a void or crack, shall not exceed 10% of the land area, or in the case of a crack or scratch, it shall not exceed more than 10% of the shortest dimension of the land.

4.5.3 An uneven land surface, *i.e.,* undulations or ripple, is acceptable provided the defect is ≤ 10 μm in height.

4.6 Wire bond pads

4.6.1 Wire bond pads shall be free of internal defects.

4.6.2 Edge defects in wire bond pads, such as nicks or edge roughness, are acceptable provided they reduce the bond pad area by no more than 20%, including reduction by over etching.

4.6.3 An uneven bond pad surface, *i.e.,* undulations or ripple, is acceptable provided the defect is ≤ 5 μm.

4.7 Though hole vias

The minimum annular ring thickness at any point on the via capture pad for through hole vias shall be ≥ 60 % of the substrate thickness. The minimum distance between the edge of the via drill and the outer edge of the capture land for a 50 μm substrate is 30 μm.

4.8 Ni/Au plating on surface mount solder lands and wire bond pads

4.8.1 Exposed Ni and/or Cu outside of the area to be soldered/wire bonded is permitted on a maximum of 1 % of the land area.

4.8.2 Discoloration shall not be a cause for rejection provided it does not interfere with solderability nor decrease the wire bond pull strength.

5 Inspection and Testing

Visual inspection, microsection inspection and electrical testing are required of all flex circuits.

5.1 Visual Inspection

Visual inspection of the flex circuits for the applicable dimensional and workmanship characteristics, as described herein and in the Fabrication Drawings (apfh5xfab.pdf), shall be under magnification of at least 10X. Higher magnification may be used as required to verify defects.

5.2 Microsection Examination

5.2.1 Microsection examination shall be performed per IPC-TM-650 method 2.1.1 or 2.1.1.2 .

5.2.2 The test coupon shall be agreed upon by the Purchaser and the Vendor.

5.2.3 A minimum of three micro-vias shall be inspected in vertical cross section.

5.2.4 The specimens shall be thermally stressed in compliance with IPC-TM-650 method 2.6.8 before microsection examination.

5.2.5 Results shall be provided in writing or electronic form with delivered flexible circuits.

5.2.6 Conductor thickness at any location shall be within the range given in the table in section 3.5 of this document.

5.2.7 Ni plating thickness at any location shall be within the range given in the table in section 3.5 of this document.

5.2.8 Au plating thickness at any location shall be within the range given in the table in section 3.5 of this document.

5.2.9 The minimum substrate thickness at any point shall be ≥ 40 μm.

5.2.10 The via hole to via capture pad alignment is given in section 4.7 of this document.

5.2.11 An offset between the top and bottom metal registration is acceptable within the limits defined by section 4.7 of this document.

5.2.12 Breakout of any via capture pad is not acceptable.

5.2.13 Via holes must be open through the entire thickness of the substrate.

5.2.14 The average thickness of Cu plating in the vias shall be ≥ 7 μm.

5.2.15 No more than one plating void per test specimen is acceptable, provided the size of the plating void is ≤ 5 % of the whole plating area and it is not located in the interconnection plating area to the target land.

5.2.16 No more than one plating void per test specimen is acceptable, provided the size of the plating void is ≤ 5 % of the whole plating area and it is not located in the interconnection plating area to the target land.

5.2.17 Plating cracks that are visible before or after thermal stressing are not acceptable.

5.3 Electrical Testing

5.3.1 Electrical testing shall be performed on all flex delivered as "Good".

5.3.2 The test voltage shall be 100 Vdc ± 20 %.

5.3.3 The test current shall be 10 mAdc ± 20 %.

5.3.4 The insulation resistance shall be >2 MΩ.

5.3.5 The continuity resistance shall be ≤ 10 Ω.

6 Rework and Repair

6.1 Conductors

6.1.1 Removal of shorts between conductors is acceptable, provided such repairs do not affect the integrity of flex circuits, as set forth in this document. .

6.1.2 Removal of residual plating material, including Cu, is acceptable, provided such repairs do not affect the integrity of flex circuits, as set forth in this document.

6.1.3 Conductor welding is not acceptable.

6.2 Solder resist/cover layers

6.2.1 Rework/touchup/repair of the bottom solder resist/cover layers is not acceptable.

6.2.2 Rework/touchup/repair of the top solder resist/cover layers is acceptable.

7 Quality Assurance

7.1 Workmanship

The boards shall be of uniform quality and free from:

- Dirt
- Oil and grease

- Corrosion
- Salt
- Fingerprints
- Foreign materials

And any other defects which might affect quality, reliability, endurance or appearance.

Cleaning and rinsing shall be performed using halogen (*e.g.*, chlorine and bromine) free products. The vendor must maintain ISO 9001 or ISO 9002 certification.

7.2 Every production lot shall be identified by a unique number which allows tracing back to the purchase order and all manufacturing documents, inspection and test reports and the batch numbers of the base materials used in construction of the flex circuits.

7.3 Final inspection

Test and inspection is to be performed as defined in section 5 of this document.

7.4 Any nonconformance observed shall with respect to the construction , physical dimensions, process parameters or test/inspection shall be recorded in the manufacturing document.

8 Delivery

8.1 Shipment shall be FOB Vendor's factory.

8.2 All shipments shall be by quickest means.

8.3 All shipments shall be insured for replacement value.

8.4 All shipments shall be addressed as follows:

Department of Physics and Astronomy
University of Oklahoma
440 West Brooks Street
Norman, OK 73019
USA
attn: Rusty Boyd

8.5 All shipments shall be conspicuously marked with the purchase order number on the outside of the packaging.

8.6 Flex circuits shall be clean and dry before packaging.

8.7 Flex circuits do not need to be individually packaged, however:

8.7.1 Each flex circuit must be physically isolated from the other flex circuits and any abrasive materials.

8.7.2 Each flex circuit must be protected from bending or creasing during shipping and unpacking.

8.7.3 Each flex circuit shall be sealed away from moisture and contamination.

8.7.4 No staples or other sharp objects are acceptable in or through the inner most layer of packaging for the flex circuits, *i.e.,* the packaging immediately in contact with the flex circuits.

8.8 The packaging shall be marked with the following:

8.8.1 Vendor's name

8.8.2 Flex circuit version number

8.8.3 Lot number

8.8.4 Manufacturing date (year and week)

8.9 Documentation

Each lot shall be accompanied by the following:

- Certification of Conformity
- Inspection Certificates of the visual (final) inspection and of the microsection inspection.
- Copies of all microsection photographs