Acceptability Criteria for DYOstrate® Micro-Via
High Density Interconnects

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DYCONEX
ADVANCED CIRCUIT TECHNOLOGY
Notice

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Change Record

This page records the changes to the specification, page 2 onwards. The area of the change is shown at each issue by a vertical line in the left hand margin.

<table>
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<th>Issue</th>
<th>Details of Change</th>
<th>Change No and Date</th>
<th>Signature</th>
</tr>
</thead>
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<tr>
<td>A</td>
<td>Initial release</td>
<td>4.11.98</td>
<td>QA/Bug</td>
</tr>
<tr>
<td>A</td>
<td>Address Change in Notice-Sheet (No Revision change, date only)</td>
<td>05.06.2002</td>
<td>QA/Bug</td>
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1 Scope
This standard covers the qualification and performance requirements of DYCOstrate® Printed Wiring Boards (PWB), High-Density-Interconnects (HDI) and Multi-Chip-Modules (MCM) utilising plasma generated micro-vias. The substrates may be single-sided, double-sided and/or multilayer with or without constrained support carrier or core (i.e. CIC, CMC, CCC, etc.).

2 Performance Classification
The printed boards are classified by the three performance classes according IPC-6011:

- Class 1: General Electronic Products
- Class 2: Dedicated Service Electronic Products
- Class 3: High Reliability Electronic Products
The required performance class shall be specified in the procurement documents.

3 Applicable Documents

3.1 International Standards
IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits
IPC-D-275 Design Standard for Rigid Printed Boards
IPC-6011 Generic Performance Specification for Printed Boards
IPC-6012 Qualification and Performance Specification for Rigid Printed Boards
IPC-6016 Qualification and Performance Specification for High Density Interconnect Structures (HDIS)
IPC-A-600 Acceptability of Printed Boards (rev. level "E" or higher)
IPC-R-700 Guideline for Modification, Rework and Repair of Printed Boards and Assemblies
MIL-P-50884 Military specification for flexible and rigid-flex printed wiring boards
MIL-P-55110 Military specification for rigid printed wiring boards

3.2 Supplementary DYCONEX Documents
DYCOstrate® Technology Information
DYCOstrate® Design Rules
DYCONEX Workmanship Standards
3.3. **Terms and Definitions**

The definition of terms herein shall be as specified in IPC-T-50 or as listed below:

**DYCOstrate®**
Brand name for PWBs, HDIs or MCMs produced by using plasma ablation technology invented and patented by Dyconex Ltd.

**Micro-Via**
General term for processed (plated or non plated) hole $\leq 150\mu m$ (0.006inch) diameter

**Blind Micro-Via**
A micro-via etched from one side of the base material extending to the next copper layer

**Through-Hole Micro-Via**
A micro-via etched from both sides of the base material interconnecting the two surfaces of a copper clad foil

**Target Land**
The land on which the micro-via ends and makes connection

**Capture Land**
The land where the micro-via starts. It may vary in shape and size based on the intended use (i.e. component mounting, via entrance conductor)

**Core**
Pre-manufactured conventional PWB (2-n layer) or electrically non-functional support carrier, constrained or unconstrained, which is laminated between the micro-via build-ups. Core material can be any appropriate material, like FR-4, FR-5, G10, etc., constraining materials can be copper-invar-copper (CIC), copper-molybdenum-copper (CMC), copper-carbon-copper (CCC), etc.
Thermal Vias
Thermal interconnection between the layers. Typically they are arranged as an array of staggered micro-vias in a larger copper pad.

Parallel Vias
The parallel micro-vias are located in the same pad which are used for mechanically drilled holes. These parallel micro-vias are used to enable electrical pre-testing of a micro-via layer build-up before final lamination and to improve the overall board reliability.

RCC
Resin-coated-copper foil (usually, non-reinforced, non-cured epoxy coated onto the back side of a copper foil)

4 Requirements
This specification describes those requirements which are not covered by the applicable international standards mentioned in paragraph 3.1 as well as any exceptions related on the DYCOstrate® technology.

References printed in *Italic* identify criteria's and requirements for the micro-via technology which deviate from the referenced paragraphs or which are derived from them.

4.1 Material

Rigid Laminates
Rigid glass-reinforced laminates, metal clad and unclad, shall be as specified in the procurement documentation and shall be selected from IPC-4101, IPC-4104 and MIL-S-13949

Flexible Films
Flexible films, metal clad and unclad, shall be as specified in the procurement documentation and shall be selected from IPC-FC-231 and IPC-FC-232

Bonding Materials
Bonding materials shall be as specified in the procurement documentation and shall be selected from IPC-FC-232 and IPC-4101 (substitute for MIL-S-13949)

Other Dielectric and Conductive Materials
Other Materials shall be as specified in the procurement documentation and shall be selected from IPC-4104

Metal Foils
Copper foil as well as resin coated copper foil (RCC) shall be selected from IPC-MF-150. Foil type, foil grade, bond enhancement treatment and foil profile should be specified in the procurement documentation

Polymer Hole Fill Material
When required, the material used for hole fill shall be in accordance with IPC-4104 or IPC-SM-840

Nickel Plating
Nickel plating shall be in accordance with QQ-N-290. If electroless plated nickel is required it shall be specified in the procurement documentation

Gold Plating
Gold plating shall be in accordance with MIL-G-45204. If electroless plated gold is required it shall be specified in the procurement documentation

Solder Mask
When permanent solder mask coating is specified, it shall according IPC-SM-840 class 3.
If flexible solder mask is required it shall be specified in the procurement documentation.

### 4.2 Construction (Build-Up)

Printed circuit boards delivered under this specification shall be of the material, design, and construction specified in the applicable procurement documentation.

### 4.3 Markings

In addition to the customer defined markings such as article number, revision level, date code, etc., DYCONEX attaches the following identification markings to the boards:

- Lot-N° (e.g. AAA, AAB, AAC ...)
- Company code "co"
- Serial-N° (e.g. 01, 02, 03 ...) if requested by the customer
- Position N° (A, B, C ...) of the boards if a production panel contains more than one board, if requested by the customer

Markings which do not vary within a production lot are usually etched in copper. Variable markings such as serial number will be stamped onto the substrates in white or black colour.

### 4.4 Dimension and Tolerances

#### 4.4.1 Board Dimensional Requirement

The board shall meet the dimensional requirements specified in the procurement documents. All dimensional characteristics such as

- board outline (contour)
- thickness
- cut-outs and slots
- fixing tabs

shall be as specified in the procurement documents.

#### 4.4.2 DYCOstrate® Technology Related Tolerances

##### 4.4.2.1 Board Contour

The tolerance of the plasma etched board contours is $\pm 200 \, \mu\text{m}$ (0.008 inch).
The tolerance of mechanically routed contours is \( \pm 100 \, \mu \text{m} \) (0.004inch).

### 4.4.2.2 Hole Pattern to Board Contour
The tolerance between plasma etched holes to the plasma etched board contour is
\[ \pm 75 \, \mu \text{m} \] (0.003inch) for 2 layer structures
\[ \pm 125 \, \mu \text{m} \] (0.005inch) for 4 layer structures.

The tolerance between plasma etched holes to the mechanically routed board contours is
\[ \pm 200 \, \mu \text{m} \] (0.008inch).

The tolerance between mechanically drilled holes to the mechanically routed board contours is
\[ \pm 200 \, \mu \text{m} \] (0.008inch).

The tolerance between mechanically drilled holes to the plasma etched board contour is
\[ \pm 200 \, \mu \text{m} \] (0.008inch).

### 4.4.2.3 Hole Pattern
The tolerance between two mechanically drilled is
\[ \pm 100 \, \mu \text{m} \] (0.004inch).
The tolerance between two plasma etched holes is 
\[ \pm 50 \, \mu m \, (0.002\text{inch}) \].

The tolerance between plasma etched holes to mechanically drilled holes is 
\[ \pm 200 \, \mu m \, (0.008\text{inch}) \].

### 4.4.2.4 Cut-outs and holes

The diameter and shape tolerance of plasma etched holes and cut-outs is 
\[ \pm 50 \, \mu m \, (0.002\text{inch}) \] on plated holes and cut-outs 
\[ \pm 75 \, \mu m \, (0.003\text{inch}) \] on non-plated holes and cut-outs

### 4.5 Visual Examination

Visual examination of the substrates for the applicable dimensional or workmanship attributes shall be conducted at a magnification of minimum 10X \( \pm 10 \% \). If the condition of a suspected defect is not apparent, it might be verified at a higher magnification (up to 40X) to confirm that is a defect.

(Reference IPC-6016, 3.5 and IPC-6012, 3.3)

#### 4.5.1 Conductor Pattern

##### 4.5.1.1 Board Edges

The minimum spacing between the conductor and the edge of the board shall be specified in the procurement documents.

(Reference IPC-6016, 3.5.3, IPC-6012, 3.5.3)

Nicks or halos on finished substrate edges shall be acceptable provided that the penetration does not bridge adjacent conductors or reduce the spacing requirements below the minimum, specified in the procurement documents.

(Reference IPC-6016, 3.3.1, IPC-6012, 3.3.1)
Non-conductive burrs along the edges of the finished board shall be acceptable as long as they are not loose and/or do not affect fit and function.

(Reference IPC-6016, 3.3.1, IPC-6012, 3.3.1)

4.5.1.2 Minimum Conductor Width

If not specified on the master drawing, the minimum conductor width (b) shall be \( \geq 80\% \) of the nominal width (a) supplied in the procurement documentation. The conductor width is measured on the bottom, where the conductor adheres to the base material.

(Reference IPC-6016, 3.5.1, IPC-6012, 3.5.1)

4.5.1.3 Reduction of the Minimum Conductor Width

An additional reduction of the minimum specified conductor width of \( \leq 20\% \), due to isolated defects (i.e. edge roughness, nicks, pinholes and scratches) is acceptable, provided the length (L) of a single defect is not longer than 13mm.

(Reference IPC-6016, 3.5.1, IPC-6012, 3.5.1)

4.5.1.4 Minimum Conductor Spacing

If not specified on the master drawing the minimum conductor spacing (b) shall be \( \geq 80\% \) of the nominal spacing (a) supplied in the procurement documentation. The conductor spacing is measured on the bottom, where the conductor adheres to the base material.

(Reference IPC-6016, 3.5.2, IPC-6012, 3.5.3)

4.5.1.5 Reduction of the Minimum Conductor Spacing

Minimum conductor spacing may be reduced by an additional \( \leq 20\% \) due to conductor edge roughness spikes, etc.

(Reference IPC-6016, 3.5.2, IPC-6012, 3.5.3 and tab. 3-6)

Remaining copper between conductors is acceptable, provided they do not reduce the minimum conductor spacing as it is defined above.

(Reference IPC-6016, 3.5.2, IPC-6012, 3.5.3 and tab. 3-6)
4.5.1.6 Surface Mount Lands

Defects such as nicks, dents etc. along the edge of a land shall not exceed 20% of either the length or width of the land.

(Reference IPC.6016, 3.5.3.2, IPC-6012, 3.5.4.2)

The maximum length of an internal defect shall not exceed 10% of the length or width of the land.

(Reference IPC-6016, 3.5.3.2, IPC-6012, 3.5.4.2)

4.5.1.7 Wire Bonding Surface

The bonding area shall be free of defects

(Reference IPC.6016, 3.5.3.3)

Edge roughness and indentations in a bonding area are acceptable as long as more than ≥75% of the wire bonding land area is undisturbed.

(Reference IPC.6016, 3.5.3.2, IPC-6012, 3.5.4.2, Martin Marietta Microelectronics Workmanship Standard 1-6)

4.5.1.8 Evenness of Surface Lands

Layout related undulated lands (uneven land surface) are acceptable up to

≤25 µm (0.001 inch) for soldering lands,

≤10 µm (0.0004 inch) for wire bonding lands

Undulated land are usually resulting from a non-optimal layout and can only be avoided by optimising the copper layer underneath the surface land.
4.5.2 **Annular Ring Requirements**

4.5.2.1. **External on Blind Micro-Vias**

The minimum annular ring for blind micro-vias shall be \( \geq 0 \text{ µm} \). That means, in minimum, the copper of the via wall plating shall be visible.

*(Reference IPC-6016, 3.4.3, IPC-6012, 3.4.3)*

![Surface view](image1)

![Microsection view](image2)

4.5.2.2. **External on Through-Hole Micro-Vias**

The minimum annular ring \( a \) for through-hole micro-vias shall be \( \geq 60 \% \) of the dielectric thickness \( b \), i.e. 30 µm (0.0012 inch) for 50 µm (0.002 inch) material.

*(Reference IPC-6016, 3.4.3, IPC-6012, 3.4.3)*

![Surface view](image3)

![Microsection view](image4)

4.5.3. **Surface Plating and Coating**

The required surface plating and coating shall be defined on the procurement documents.

4.5.3.1. **Solder Coating Coverage**

If solder coating is required, it shall be performed by Hot-Air-Levelling (HASL). The solder coating shall completely cover the exposed conductor pattern and shall meet the solderability requirement of J-STD-003. There is no specific thickness requirement to be met.

*(Reference IPC-6012, 3.2.6.4 & table 3-2)*
4.5.3.2. Nickel / Gold Plating on Soldering Lands

If nickel/gold plating is required for soldering purpose, chemically (electroless) deposited nickel/gold shall be used. Unless otherwise specified in the procurement documents the plating thickness shall be as stated in paragraph 4.6.2.2. of this specification.

Exposed nickel and/or copper on areas not to be soldered is permitted on maximum 1 % of the conductor surface (Class 1 and 2 up to 5 %).

→ See rework possibility in Paragraph 4.8

(Reference IPC-6012, 3.5.4.6)

Discoloration shall not be a cause for rejection, provided it does not adversely affecting solderability.

4.5.3.3. Nickel / Gold Plating on Wire Bonding Lands

The nickel/gold plating for wire bonding purpose shall be specified in the procurement documents. Unless otherwise specified, the plating thickness shall be as stated in paragraph 4.6.2.2. of this specification.

Exposed nickel and/or copper outside of the bonding area is permitted on maximum 1 % of the land area (Class 1 and 2 up to 5 %).

(Reference IPC-6012, 3.5.4.6)

Discoloration shall not be a cause for rejection provided it does not adversely affect bond pull strength.

(Reference IPC-6012, 3.5.4.6)
4.5.3.4. Plating Voids in Blind Micro-Vias

Plating voids in the hole are not acceptable (see microsection requirements)

(Reference IPC-6012, 3.3.3 & Table 3-3)

4.5.3.5. Coating Voids in Blind Micro-Vias

Missing nickel / gold plating shall not exceed one void per hole in not more than 5% of the holes (see 4.6 Microsection Requirements)

(Reference IPC-6012, 3.3.3 & Table 3-3)

4.5.4. Solder Resist

4.5.4.1. Solder Resist Thickness

Depending on the type of solder resist used, the solder resist thickness may vary considerably. However, a good coverage of the board surface is required. The solder resist thickness is not measured, unless specified in the procurement documents.

(Reference IPC-6012, 3.8.3)

4.5.4.2. Solder Resist Misalignment

SMD-lands as well as bonding lands shall be free of solder resist. Encroachment of solder resist over lands due to misalignment is acceptable up to

$\leq 50 \mu m$ (0.002inch) for a pitch of $>1.25mm$ (0.05inch)

$\leq 25 \mu m$ (0.001inch) for a pitch of $<1.25mm$ (0.05inch)

(Reference IPC-6012, 3.8.1e & f)

Misalignment of solder resist shall not expose adjacent isolated lands or conductors.

→ See rework possibility in Paragraph 4.8

(Reference IPC-6012, 3.8.1e & f)
4.5.4.3. Solder Resist Coverage

Pits and voids are allowed in the non-conductor area

⇒ See rework possibility in Paragraph 4.8

(Reference IPC-6012, 3.8.1h)

Air entrapment in blind micro-vias covered with solder resist is acceptable.

(Reference IPC-6012, 3.8.1)

Micro-vias which are not or insufficiently covered by solder resist are acceptable, provided the number of affected via holes does not exceed ≤5 % of the total number of via holes per board.

(Reference IPC-6012, 3.8.1)
4.5.4.4. Coverage Between Closely Spaced Lands
Solder resist coverage between closely spaced lands requires to provide a sufficient width of solder resist already in the design. In case where the designed minimum width is \( \leq 150 \mu m \) (0.006 inch), a solder resist breakout on the finished board shall not be a cause for rejection.
(Reference IPC-6012, 3.8.1i)

4.6. Microsection Examination
Microsection shall be accomplished per IPC-TM-650, method 2.1.1 or 2.1.1.2 on test specimens, test coupons or production boards (see chapter 6.5). A minimum of three holes or micro-vias shall be inspected in the vertical cross section.

When examined in microsection the coupons shall meet the requirement of the sections 4.6.1 through 4.6.4.
(Reference IPC-6012, 3.6.1 & 3.6.2)

4.6.1. Thermal Stress Testing (Solder Float)
Specimens shall be thermally stressed in accordance with IPC-TM-650, method 2.6.8.
Following stress, the specimens shall be microsectioned.
(Reference IPC-6012, 3.6.1)

4.6.2. Board Build-Up Requirements

4.6.2.1. Conductor Thickness
The minimum external conductor thickness shall be in accordance with the nominal thickness specified in the procurement documents (copper foil plus copper plating).
(Reference IPC-6012, 3.5.2, 3.6.2.12 & Table 3-9)

Allowable reduction of the minimum external conductor thickness due to isolated defects (i.e. edge roughness, nicks, pinholes, depressions and scratches) shall not exceed 20% of the minimum conductor thickness.
(Reference IPC-6016, 3.6.1.4, IPC-6012, 3.5.2)
The minimum internal conductor thickness after processing shall be ≥ 70 % of the nominal conductor thickness specified in the procurement documents (copper foil plus copper plating).

(Reference IPC-6012, 3.6.2.11 & Table 3-8)

Allowable reduction of the minimum conductor thickness due to isolated defects (i.e. edge roughness, nicks, pinholes, depressions and scratches) shall not exceed 20 % of the minimum conductor thickness.

(Reference IPC-6012, 3.5.2)

4.6.2.2. Nickel / Gold Plating Thickness

Nickel plating used as a diffusion barrier between copper and gold shall have a minimum thickness of

≥1.3µm (50 micro-inch) for soldering lands
≥2.5µm (100 micro-inch) for wire bonding lands

(Reference IPC-6012, 3.2.6.5 & Table 3-2)

Gold plating on soldering lands shall have a thickness between 0.05µm (2 micro-inch) and 0.2µm (8 micro-inch)

The necessary thickness of gold plating on the wire bonding lands depends on the bonding method to be used. Therefore, the thickness requirement shall be specified in the procurement documentation.

(Reference IPC-6012, 3.2.6.5 & Table 3-2)

4.6.2.3. Minimum Dielectric Thickness

The minimum dielectric thickness between layers connected by blind micro-vias shall be ≥25 µm (0.001inch) unless otherwise specified in the procurement documents.

(for RCC-Foil ≥ 15 µm (0.0006inch))

(Reference IPC-6016, 3.6.1.5, IPC-6012, 3.6.2.14)

The minimum dielectric thickness between layers connected by through-hole micro-vias shall be

≥20 µm (0.0008inch) with base material of 25 µm nominal thickness
≥40 µm (0.0016inch) with base material of 50 µm nominal thickness

(Reference IPC-6012, 3.6.2.14)
4.6.2.4. Resin Fill of Micro-Vias
Buried micro-vias shall be at least 60 % filled with resin.
(Reference IPC-6012, 3.6.2.15)

4.6.3. Blind Micro-Vias

4.6.3.1. Annular Ring External (Blind Micro-Vias)
The minimum annular ring for blind micro-vias shall be ≥0 μm. That means, in minimum the copper of the via wall plating must be visible.
(Reference IPC-6016, 3.4.3 and IPC-6012, 3.4.3)

4.6.3.2. Annular Ring Internal (Blind Micro-Vias)
The minimum annular ring for blind micro-vias on internal layers shall be ≥0 μm. That means, the bottom of the micro via must be located within the target land.
(Reference IPC-6016, 3.4.2 and IPC-6012, 3.4.2)
4.6.3.3. Minimum Hole Diameter of Blind Micro-Vias
The minimum hole diameter of a blind micro-via on the bottom (b) shall be $\geq 50 \ \mu m$ (0.002 inch).

4.6.3.4. Misalignment against Target Land
Misalignment of the blind micro-via against the target land is not acceptable.

4.6.3.5. Copper Plating of Blind Micro-Vias
The average thickness of the copper plating shall be $\geq 7 \ \mu m$. The minimum thickness shall be $\geq 5 \ \mu m$ (0.0002 inch).

Copper foil overhang or “bottle necking” is acceptable, provided the copper thickness of the hole plating as well as Ni/Au coating thickness (if applicable) is not reduced below the specified minimum thickness and the micro-via is not placed within a solder pad.

A reduction of the target land’s copper thickness is acceptable, provided the total copper thickness (target land plus hole plating) is not less than $\geq 70 \ %$ of the specified copper thickness for the target land.

The minimum plated interconnection area (a) between a micro-via and the target land shall have a diameter of $\geq 50 \ \mu m$ (0.002 inch).
The filling of blind micro-vias by plated copper is acceptable.

(Dyconex)

4.6.3.6. Plating Voids in Blind Micro-Vias

No more than one plating void per test coupon is acceptable provided the size of the plating void is ≤5 % of the whole plating area. The test coupon has to be agreed between the customer and Dyconex.

(Reference IPC-6012, 3.6.2.2)

4.6.3.7. Plating Cracks in Blind Micro-Vias

Plating cracks visible before or after solder-float testing are not acceptable.

(Reference IPC-6012, 3.6.2.1)

4.6.3.8. Nickel / Gold Plating Voids in the Hole

Missing nickel / gold plating shall not exceed one void per hole in not more than 5 % of the total number of holes on the board.

(Reference IPC-6012, 3.3.3 & Table 3-3)

4.6.3.9. Nickel / Gold Plating over Copper Plating Void

Acceptable, provided, the minimum copper thickness underneath the Ni/Au plating is ≥5 μm (0.0002inch).

(Reference IPC-6012, 3.3.3 & Table 3-3)
4.6.4. **Trough-Hole Micro-Vias**

4.6.4.1. **Annular Ring (Through-Hole Micro-Vias)**

The minimum annular ring \(a\) for through-hole micro-vias shall be \( \geq 60\% \) of the dielectric thickness \(b\), i.e. 30\(\mu\)m (0.0012\text{inch}) for 50\(\mu\)m (0.002\text{inch}) dielectric material.

(Reference IPC-6016, 3.4.2 and IPC-6012, 3.4.2)

4.6.4.2. **Misalignment**

An offset between the top-side against the bottom-side is acceptable, provided the plating- and annular ring requirements are met.

(Reference IPC-6016, 3.4.3)

4.6.4.3. **Hole Break-Through**

Break-through of the hole, caused by excessive plasma etching and/or misalignment is not acceptable

(Dyconex)
4.6.4.4.   Non-Open Holes (Through-Hole Micro-Vias)
Too short plasma etching is acceptable provided the plated through-hole is still open and the plating
requirements are met. The closing of micro-vias by copper plating is not acceptable.

(Dyconex)

4.6.4.5.   Copper Plating of Through-Hole Micro-Vias
The average thickness of the copper plating shall be ≥7 µm. The minimum thickness shall be ≥5 µm (0.0002inch)
(Reference IPC-6012, 3.6.2.10 & Table 3-2)

4.6.4.6.   Plating Voids in Through-Hole Micro-Vias
No more than one plating void per test specimen is acceptable, provided the size of the plating void is ≤ 5 % of the whole plating
area, and it is not located in the interconnection plating area to the target land. The test coupon has to be agreed between the customer
and Dyconex.
(Reference IPC-6012, 3.6.2.2)

4.6.4.7.   Plating Cracks in Through-Hole Micro-Vias
Plating cracks visible before or after solder-float testing in are not acceptable.
(Reference IPC-6012, 3.6.2.1)

4.6.4.8.   Nickel / Gold Plating Voids in the Hole
Missing nickel / gold plating shall not exceed one void per hole in not more than 5 % of the total number of holes on the board.
(Reference IPC-6012, 3.3.3 & Table 3-3)
4.6.4.9. Nickel / Gold Plating over Copper Plating Void

Acceptable, provided the minimum copper thickness underneath the Ni/Au plating is \( \geq 5 \, \mu m \) (0.0002inch).

(Reference IPC-6012, 3.3.3 & Table 3-3)

4.6.5. Special Purpose Micro-Vias

4.6.5.1. Parallel Micro-Vias

Since the parallel micro-vias provide additional current paths parallel to a mechanically drilled plated through-hole, some defects (as described below) can be tolerated without any influence to fit, form and function.

Parallel micro-vias cut by the mechanically drilled hole (due to misalignment) shall be acceptable

(Dyconex)

Plating defects in no more than \( \leq 50 \% \) of the parallel micro-vias (due to misalignment) shall be acceptable, provided that the plating of the mechanically drilled holes still complies to the specification.

(Dyconex)
Plating defects in the mechanically drilled holes such as inner layer separation or plating voids, shall be acceptable, provided that the corresponding parallel micro-vias do not show plating defects as well.

(Dyconex)

Plating defects such as inner layer separation or missing plating in areas of the copper barrel, which have no redundant parallel micro-vias (core area), are not acceptable.

(Dyconex)

4.6.5.2. Thermal Micro-Vias
Thermal micro-vias have no electrical function. Therefore, thermal micro-vias are not subject to any evaluation.

4.7. Electrical Testing
The testability as well as the applicable test parameters depend on the structure, density and the size of the substrate to be tested.

Unless otherwise specified in the procurement document, electrical testing will be carried out as follows:

<table>
<thead>
<tr>
<th>Standard Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Voltage</td>
</tr>
<tr>
<td>Test Current</td>
</tr>
<tr>
<td>Insulation Resistance</td>
</tr>
<tr>
<td>Continuity Resistance</td>
</tr>
</tbody>
</table>
4.8. **Rework and Repair**

Exposed nickel and/or copper areas in soldering pads (i.e. SMD lands, etc.) affecting not more than 3 % of the total number of solder pads may be reworked by manual tinning.

**Touch-up of solder** resist discontinuities shall be allowed, provided that the end product meets the other solder resist requirements.

(Reference IPC-SM-840, 3.4.9)

**Conductor welding** on inner layers shall be accepted, providing there are no more than 3 places with a max. length of ≤5 mm on a board. The welding shall be performed and inspected per IPC-R-700 (4.2.5). The weld repair shall not reduce the minimum electrical space requirements.

(Reference IPC-6012, 3.12.1)
Conductor welding on surface layers shall be accepted, providing there are no more than \( \leq 3 \) places with a max. length of \( \leq 5 \text{ mm} \) on a board. The welding shall be performed and inspected per IPC-R-700 (4.2.5). The weld repair area must be covered with an appropriate epoxy coating.

(Reference IPC-6012, 3.12.1)

Removal of residual plating materials or extraneous copper is permitted, provided such action does not affect the functional integrity of the board (see IPC-R-700).

(Reference IPC-6012, 3.12)

5. Workmanship
The boards shall be uniform in quality and free from
- dirt
- oil
- corrosion
- salt grease fingerprints
- foreign materials
- and any other defects
which may affect quality, reliability, endurance and appearance.
Acceptance / reject requirements which are not listed herein or in the IPC-A-600, especially the DYCOstrate® and Micro-via related criteria, will be specified in the **DYCONEX Workmanship Standard**.

The purpose of the DYCONEX Workmanship Standard is to clarify the acceptance and rejection criteria for workmanship, where the basic measure of quality is largely subjective. Clarification is accomplished through the use of photographs which show examples of common workmanship cases ranging from perfect to rejectable.

### 6. Quality Assurance

#### 6.1. Quality Assurance and Inspection System

DYCONEX maintains an established Quality Management System according to ISO-9002 which is certified by BVQI since 1993. Survey audits are being performed every six month by the certification body.

#### 6.2. Traceability

Every production lot is identified by a unique Lot-Number (i.e. AAA, AAB, etc.) which allows to trace back to the purchase order, all manufacturing documents, all inspection and test reports as well as the batch number of the base materials used. Where appropriate, the single boards are identified by a serial number.

#### 6.3. Final Inspection

Prior to release for shipment all boards are being subjected to a final inspection including:

- Visual inspection
- Dimensional inspection
- Microsection evaluation (one test coupon per panel)
- Electrical test (100 %)

#### 6.4. Non-Conformance

Any non-conformance that is observed in respect of the process, design, construction, physical dimensions or tests will be recorded in the manufacturing document file.

#### 6.5. Test Coupons

Unless otherwise specified by the customer, Dyconex uses the Dyconex-Standard Test Coupons which represent the relevant hole configuration of the board and contain all types of micro-vias and mechanically drilled holes.
7. **Preparation for Delivery**

7.1. **Packing**

In order to prevent damages to the boards they shall be cleaned, dried and individually packed in vacuum sealed polyethylene- or aluminium bags.

The requirement for packing (type of bag, number of boards per bag) shall be as specified in the procurement documents.

The bags are marked with a label containing the following information:

- Suppliers name
- Item identification
- Lot- and serial number of the board
- Manufacturing date (year and week e.g. 9834)

7.2. **Documentation**

Each lot will be accompanied by the following:

- Certification of Conformity (CoC) (if requested)
- Inspection Certificates of the visual (final) inspection and of the microsection inspection,
- Test coupons (as required by the customer),
- One microsection sample.