Flex Circuits for the ATLAS Pixel Detector

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Abstract

Recent progress on designs of low-mass, flexible circuits for the ATLAS pixel detector will be discussed. Thin flexible circuits can be used to provide power and signal connections between front-end readout chips and data acquisition chips on the 2 cm by 6 cm ATLAS pixel detector module. Layouts and SPICE simulations will be presented for such circuits based on non-standard printed circuit board design rules. Test results from circuits fabricated for other applications using similar design rules will also be presented.

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1 Introduction

An array of hybrid pixel detectors is being developed for use at the Large Hadron Collider (LHC) by the ATLAS collaboration. The detector layout consists of three barrel layers, and five disk layers at each end. Each pixel module has sixteen front-end (FE) chips bump-bonded to a single sensor. One module design option utilizes a thin flexible circuit (Flex Hybrid) which is mounted on the back of the sensor to provide interconnections for power and digital signals between the FE chips, a Module Clock and Control chip (MCC), and an optical link which are mounted on it. Wire bond pads on the edge of the hybrid will be used to connect power and signal lines to corresponding wire bond pads located on the FE chips, which extend beyond the edge of the sensor. The module is 2.14 cm wide and 6.24 cm long. This conceptual module design is illustrated in Figure 1. Several possible designs for the Flex Hybrid are presented here along with results of simulations of expected performance.

2 Flex Hybrid Designs

Minimizing mass in the active tracking volume is of crucial importance in obtaining the optimum physics performance of the ATLAS detector. We are therefore required to use thin (flexible) substrate and metal layers in design of the Flex Hybrid. Flexible printed circuit technology typically uses film substrates such as Kapton with a minimum thickness of 25 μm containing patterned surface metal layers with or without cover insulating layers (passivation). Plated through via's can be used to connect traces in different layers. Many vendors use "standard" design rules allowing minimum trace widths

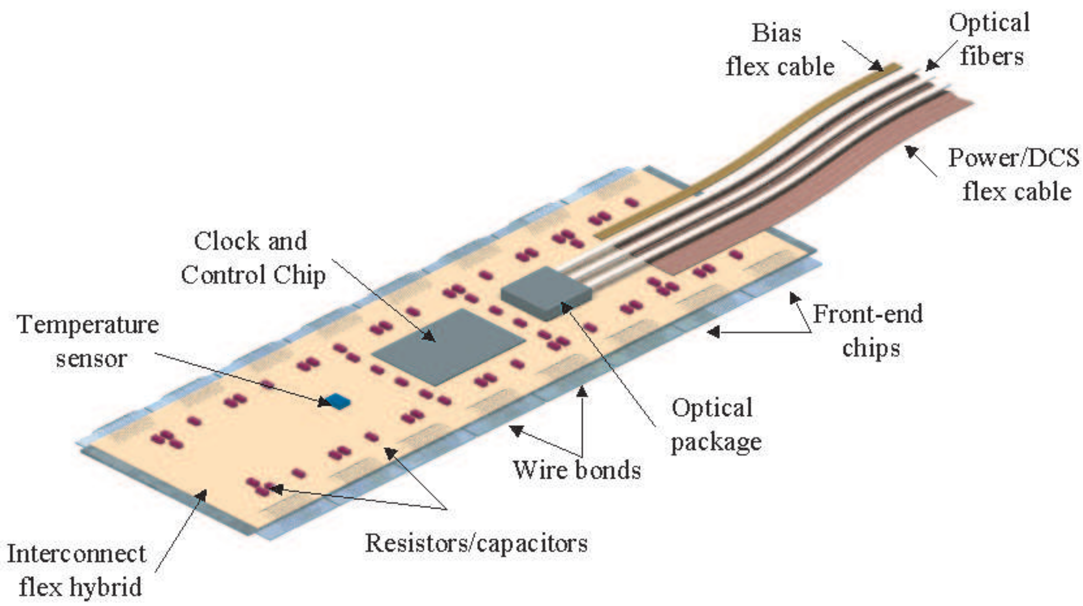

Fig. 1. Conceptual design for an ATLAS pixel module. The module is 2.14 cm wide and 6.24 cm long.

and spaces of $100\ \mu m$, $400\ \mu m$ via cover pads, and $200\ \mu m$ via through holes. Several vendors have developed High Density Interconnect (HDI) processes which can attain smaller feature sizes. For example the General Electric Corporate Research and Development (GECRD) HDI process can achieve 30 μm trace widths and spaces, 75 μm via cover pads, and 25 μm via through holes.

In the designs to be described here, the optical link has been replaced by an off-module Ladder Control Chip (LCC). The required signal and power connections between the FE chips, the MCC chip, and the LCC which are provided by the Flex Hybrid are illustrated in Figure 2. Low Voltage Differential (LVD) lines are used for the digital signals. “Broadside coupled” lines

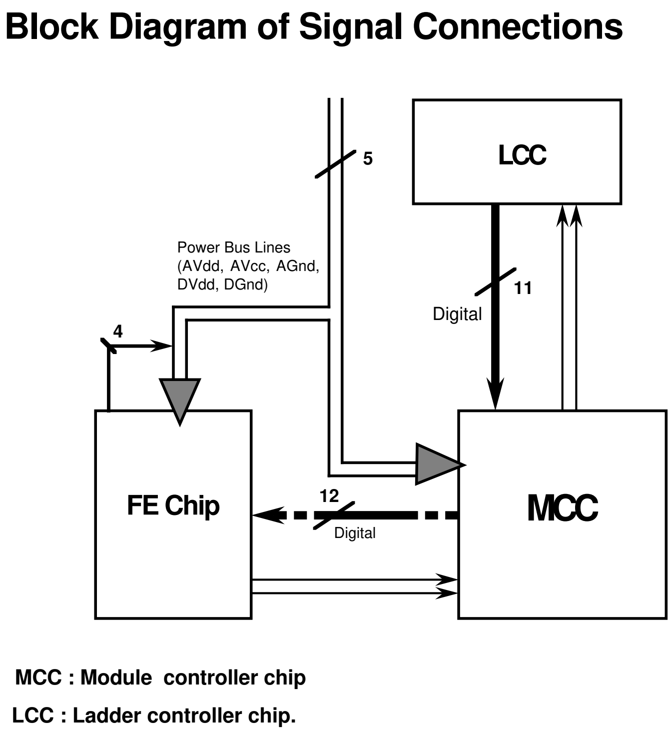

Fig. 2. Block diagram showing the signal and power connections required to be made by the Flex Hybrid.

with paired differential signals on opposite sides of a substrate layer were used whenever possible, particularly in designs using the standard design rules. In designs using HDI rules, it was often necessary to use co-planar paired differential lines in order to minimize the number of metal layers. The maximum current specifications for the FE chips were 25 mA for 3 V analog power, 50 mA for 1.5 V analog power, and 30 mA for 3 V digital power. The maximum current specification for the MCC chip was 100 mA for 3 V digital power. A maximum voltage drop of 100 mV was allowed in the power (and ground) lines over the length of the module.

The LHC beam crossing frequency is 40 MHz which is also the clock frequency for the pixel readout chips. Typical 40 MHz square waves have large-amplitude frequency components near 40, 80, and 120 MHz with smaller components at higher harmonic frequencies, so crosstalk and attenuation must be minimized for frequencies up to several hundred MHz.

A complete layout was done assuming prototype (demonstrator) designs for the FE and MCC chips using standard design rules. (It is also based on an older module design which had 12 FE chips per disk module.) It was found that six metal layers were required to make the necessary connections. This hybrid was over 300 μm thick and did not meet the material budget constraints for the pixel module. We were then motivated to use a two-piece approach in which routing near the MCC is done on a separate flex circuit called the MCC Mount (MCCM) using the HDI rules. The MCCM is then mounted on a Flex Hybrid which is designed using standard rules. This approach has the advantage that each flex circuit required only two metal layers and the overlap area is minimized. Wire bond connections must be made to connect the two flex circuits. The layout of the Flex Hybrid is shown in Figure 3 and the layout of the MCCM is shown in Figure 4.

3 Performance Simulations

To estimate the performance of the flex hybrid designs, a transmission line analysis including calculation of attenuation and crosstalk was performed using the commercial software package Maxwell Spicelink [1]. This package does a finite-element calculation of electric and magnetic fields using the multipole method in order to extract the resistance, capacitance, and inductance of conductive circuit elements. The RCL values obtained can then be loaded into SPICE so that the circuit performance can be simulated.

In order to verify this method, a simulation was first done on an existing flex circuit of relatively simple geometry which was developed for the CLEO III

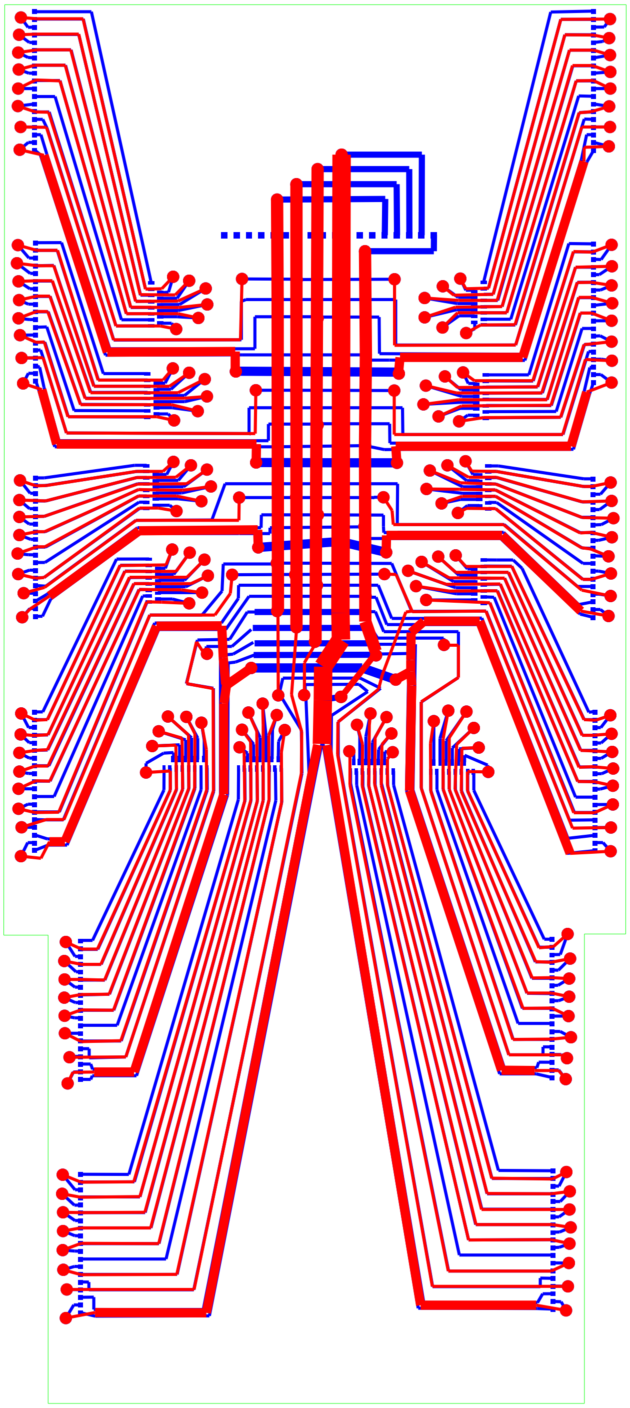

Fig. 3. Layout of the two metal layer Flex Hybrid using standard design rules.

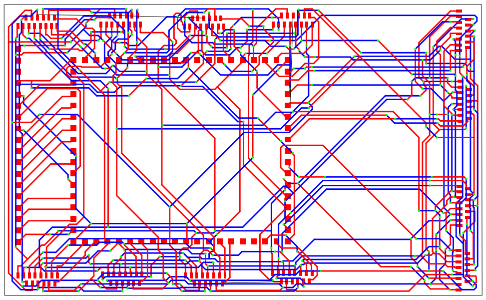

Fig. 4. Layout of the two metal layer MCCM using HDI (GECRD) design rules.

silicon microstrip detector [2]. We have established a collaboration between the University of Oklahoma and GECRD to develop the CLEO III flex circuits based on their existing high density interconnect process [3]. The flex design uses two metal layers patterned with traces on either side of a 25 μm Kapton substrate. Each side is coated with a layer of acrylic passivation 12.5 μm thick except for the area on top where wire bond pads are located. Traces are 30 μm wide and are made of 6 μm of Cu, 0.7 μm of Ni, and have 1.0 μm Au plating. A thin layer of Ti is sputtered on the Kapton before the Cu is applied to improve the adhesion of the Cu layer. The top layer (defined by the presence of bond pads) has 255 traces and the bottom layer has 256 traces. Via's with 25 μm square plated-through holes and 75 μm square cover pads are used to connect the bottom traces to bond pads on the top side. Bond pads are typically 170 μm x 60 μm.

The process, which is proprietary, uses a direct-write laser rather than conventional lithography to expose resist and thereby form the patterns. The laser is also used to construct the via holes through layers of Kapton. The total trace capacitance has been measured to be < 1 pF/cm and the trace resistance has been measured to be $< 1.2\ \Omega$/cm. The rate for defects such as non-continuous traces and shorts has been determined to be $< 0.1\%$ of all traces with about 50% of the circuits containing no defects [4]. Wire bonding

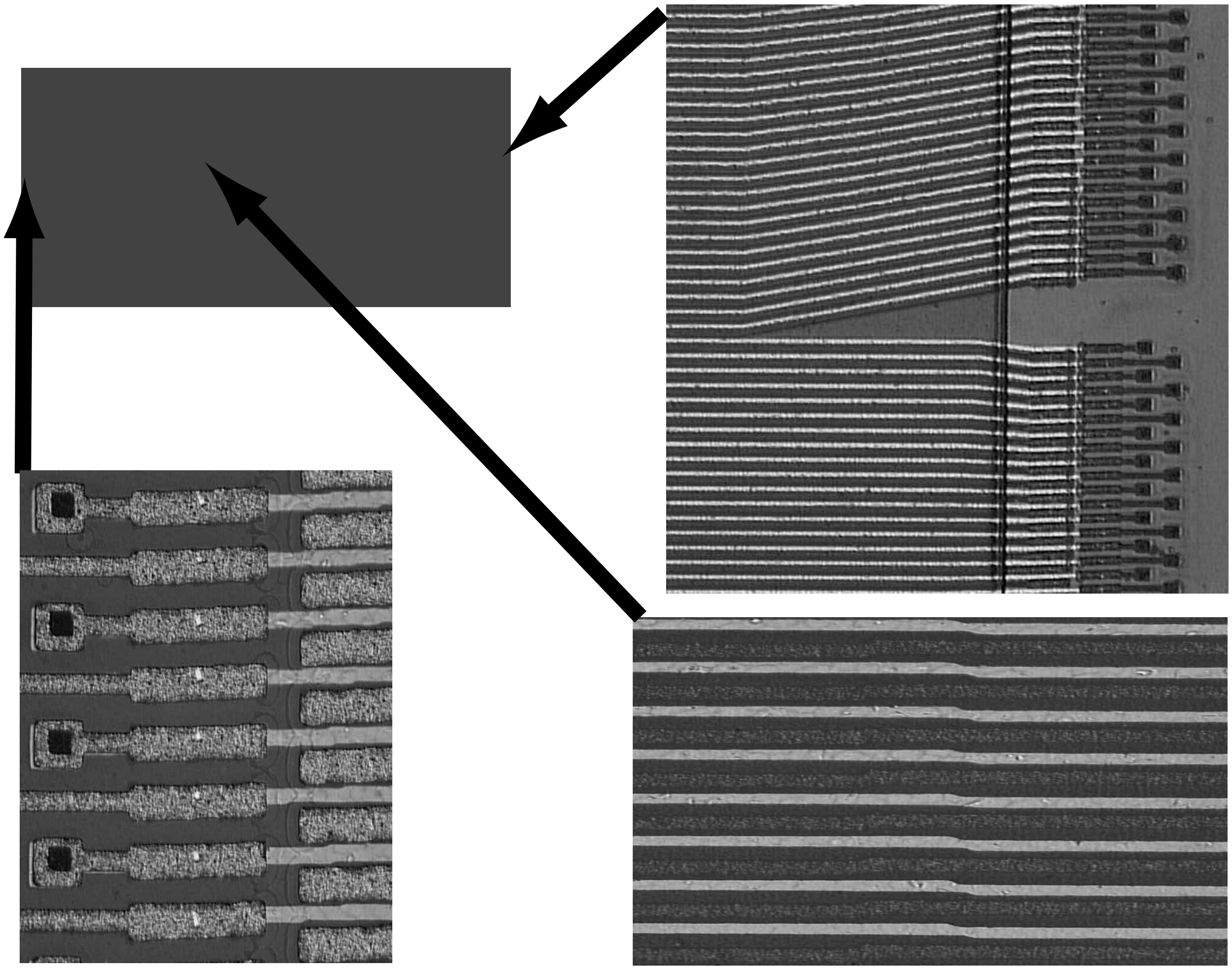

Fig. 5. Photographs of several key regions of a CLEO III production flex circuit.

to the flex circuits can be done easily with reasonable pull-strengths. The flex circuits are fabricated in a “frame” consisting of a single layer of Kapton stretched over a 17.5 cm inner diameter metal ring. A typical production flex circuit is shown in Figure 5. This process meets all the requirements for fabrication of the ATLAS MCCM design.

Simulation of the transmission line properties of a portion (up to seven traces) of the CLEO III flex circuit was done using the Maxwell Spicelink package and the results were compared to measurements. The method and results are described in detail in Ref. [5]. The Maxwell Extractor uses finite element analysis and the multipole method to extract RCL matrices for 3-dimensional structures and discontinuities. The extracted quantities can be exported directly in matrix format, or can be used to automatically generate SPICE models. In the simulation, a square wave clock signal with 2 ns rise and fall times was used as input to one ("active") trace. The attenuation (output voltage/input voltage) on opposite ends of the active trace and crosstalk (output voltage on neighboring trace/input voltage on active trace) were determined from the SPICE simulations as a function of clock pulse frequency. All traces were terminated by 50 Ω resistors although the expected characteristic impedance of the CLEO III geometry is expected to be $> 150\ \Omega$. This mismatch in impedance made the crosstalk and attenuation larger and easier to measure.

The attenuation and crosstalk were measured using a microprobe station and an HP 4194A impedance phase/gain analyzer. The measurements were dominated by noise for frequencies below 100 Hz and above 10 MHz. Figure 6 shows the minimum portion on the CLEO III flex circuit used in the simulations. Figure 7 shows the attenuation (in decibels) obtained from the simulations and Figure 8 shows the crosstalk on the nearest neighbor on the opposite side of the flex circuit. The X's in Figures 7 and 8 show the results of the measurements. Reasonable agreement is obtained between the simulations and measurements for frequencies between 100 Hz and 1 MHz where the measurements are most reliable.

Sections of the Flex Hybrid and MCCM designs were also simulated using the same methods as for the CLEO III flex circuit. A typical section of the Flex Hybrid is shown in Figure 9. In this case, LVD signal high is applied to

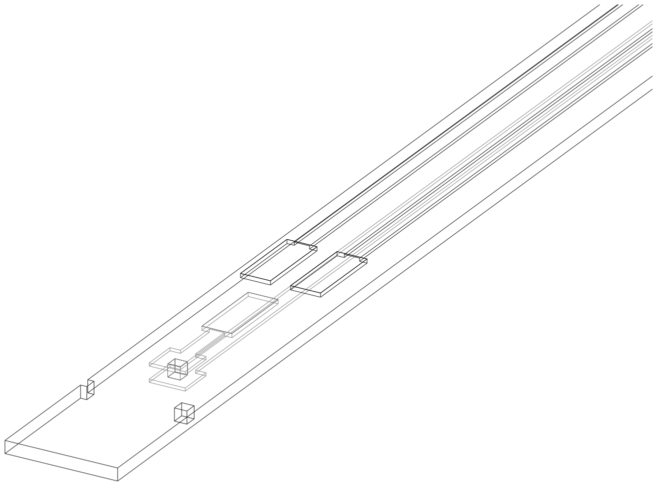

Fig. 6. The minimum portion on the CLEO III flex circuit used in the simulations.

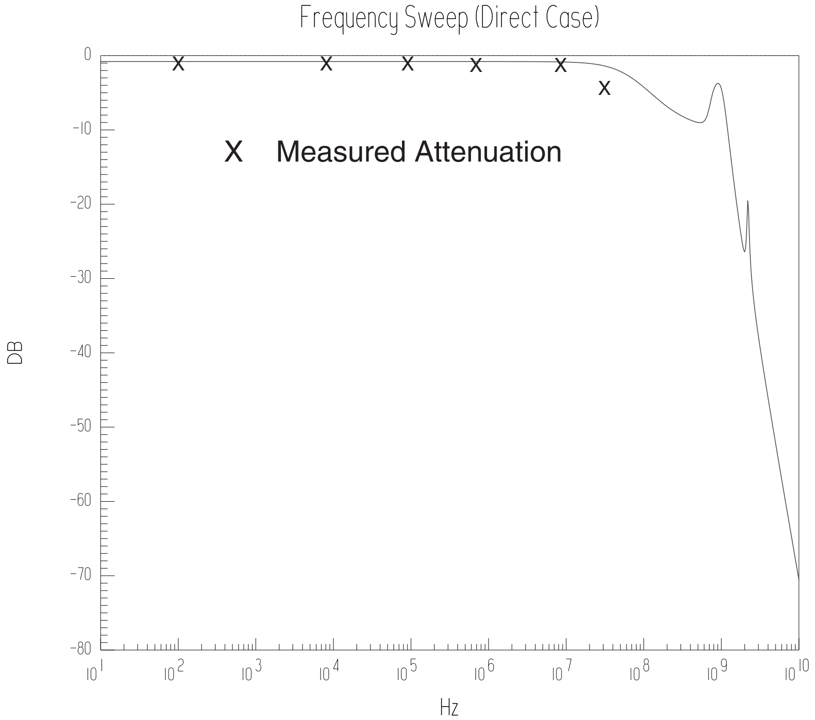

Fig. 7. The attenuation obtained from the simulations. The X's show the results of measurements.

the active trace and LVD signal low is applied to the trace on the opposite side of the two layer Flex hybrid. All traces are assumed to be terminated with 100 Ω resistors at both ends. Typical simulation results for the input and output (on opposite ends) for a 40 MHz clock pulse for signal high are

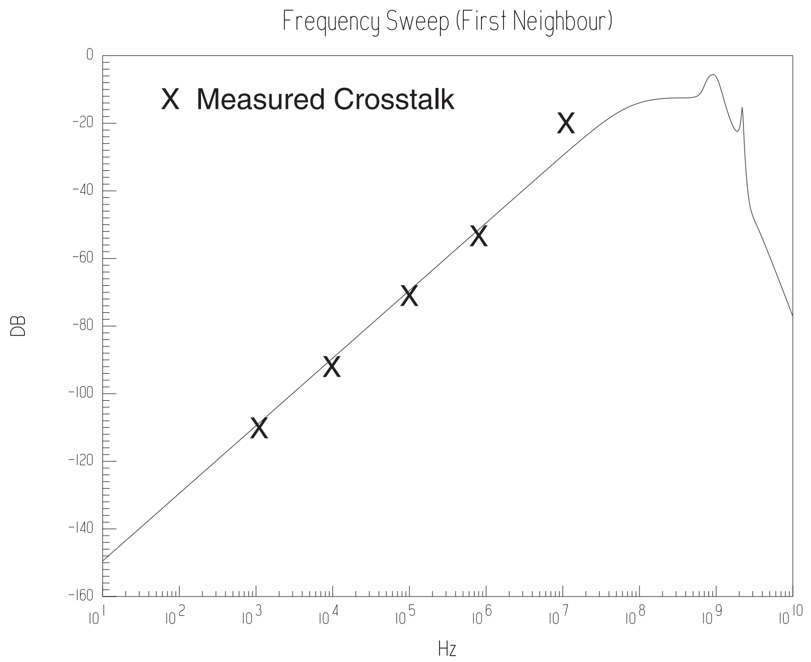

Fig. 8. The crosstalk on the nearest neighbor trace on the opposite side obtained from the simulations. The X's show the results of measurements.

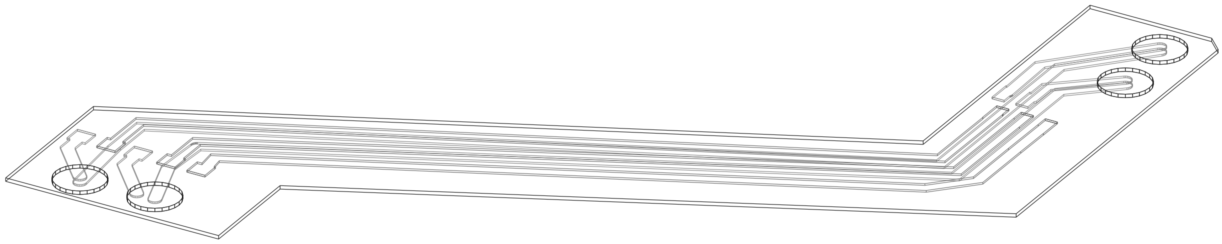

Fig. 9. A typical section of the two metal layer Flex Hybrid used in the simulations.

shown in Figure 10. The frequency dependence of the crosstalk on the nearest neighbor (same side) trace is shown in Figure 11.

A typical section of the MCCM is shown in Figure 12. Square wave clock signals were applied to the LVD high and low signal pairs as in the case of the Flex Hybrid. The MCCM has mostly co-planar LVD lines. Simulation results for the attenuation and nearest neighbor crosstalk as functions of frequency are shown in Figure 13. Figure 14 shows the phase change relative to the

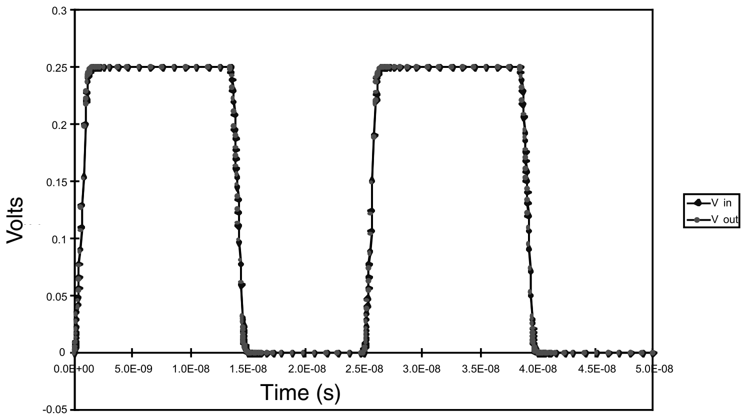

Fig. 10. Simulation results for the input and output (on opposite ends) for a 40 MHz clock pulse for LVD signal high on a Flex Hybrid trace.

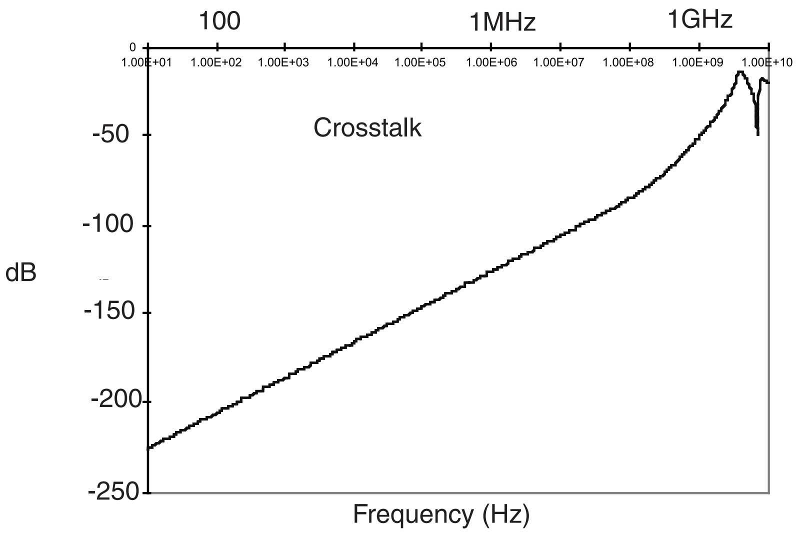

Fig. 11. Simulation result for the frequency dependence of the crosstalk on the nearest neighbor Flex Hybrid trace for LVD signal high.

generated clock phase for the active and crosstalk signals versus frequency. A large variation of phase change is observed above 5 GHz when the wavelength of the input pulse approaches twice the length of the trace as expected. Qualitatively similar results are obtained when portions of the Flex Hybrid and

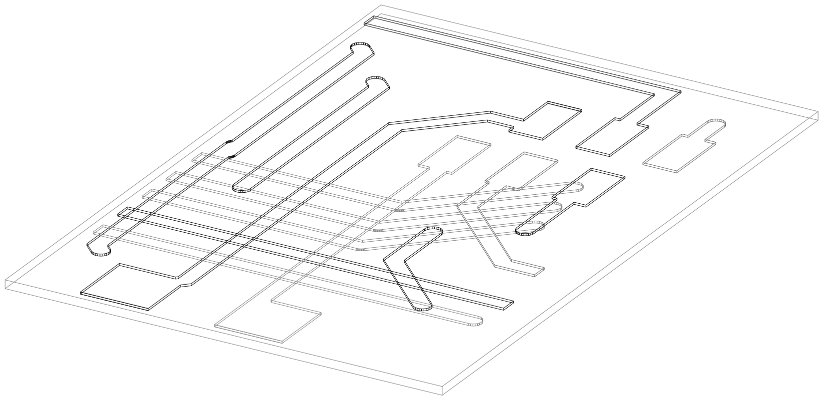

Fig. 12. A typical section of the two metal layer MCCM used in the simulations.

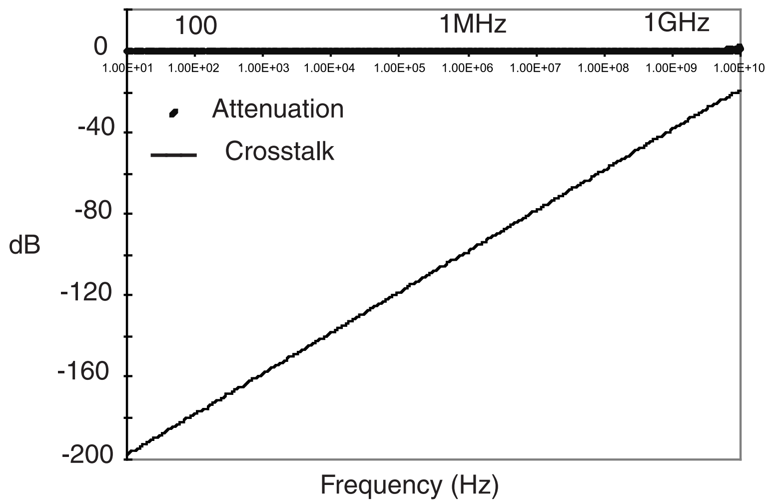

Fig. 13. Simulation results for the frequency dependence of the attenuation of the MCCM active trace and crosstalk on the nearest neighbor trace for LVD signal high.

MCCM are simulated simultaneously.

The simulation results for the two layer Flex Hybrid and MCCM show that the crosstalk on the nearest neighbor is less than -40 dB at 1 GHz and less than -60 dB at 40 MHz. Signal attenuation is negligible up to 500 MHz. Encouraged by these results, we have designed a prototype Flex Hybrid for fabrication as described in the next section. Evolution of the disk mechanical

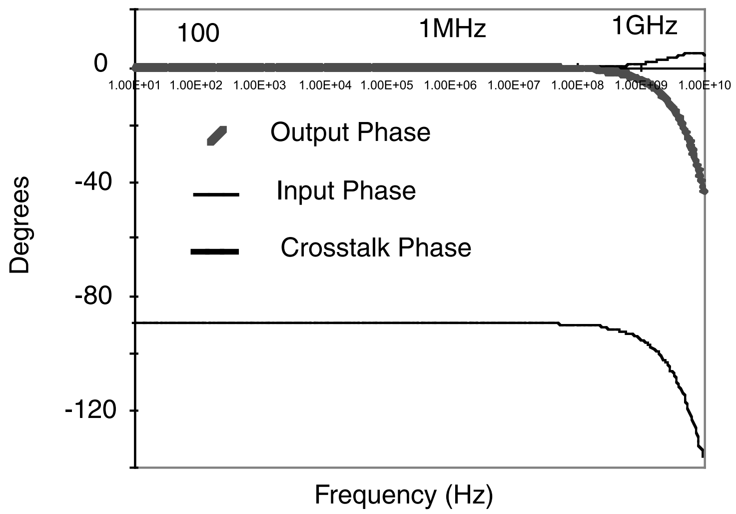

Fig. 14. Simulation results for the frequency dependence of the phase change of the MCCM active trace and the nearest neighbor trace for LVD signal high.

design has led to a solution which allows the same pixel module to be used in both the barrel and disk regions. The two metal layer monolithic Flex Hybrid described below can be used on this pixel module which was shown in Figure 1.

4 ATLAS Prototype Flex Hybrid

A prototype hybrid has been designed which will allow performance tests to be made in the CERN test beam. The prototype hybrid consists of a Kapton substrate with a thickness between 25 and 50 μm and with metal traces on both sides. Signal and power lines connect the wire bond pads at the edge of the module to wire bond pads near the MCC. The bottom traces are connected to the traces and bond pads on top with via's which have 70 μm diameter holes and 130 μm diameter cover pads. Both sides of the hybrid can be covered with a passivation layer except for the areas where bond pads are located. Power and ground lines as well as differential signal lines are placed

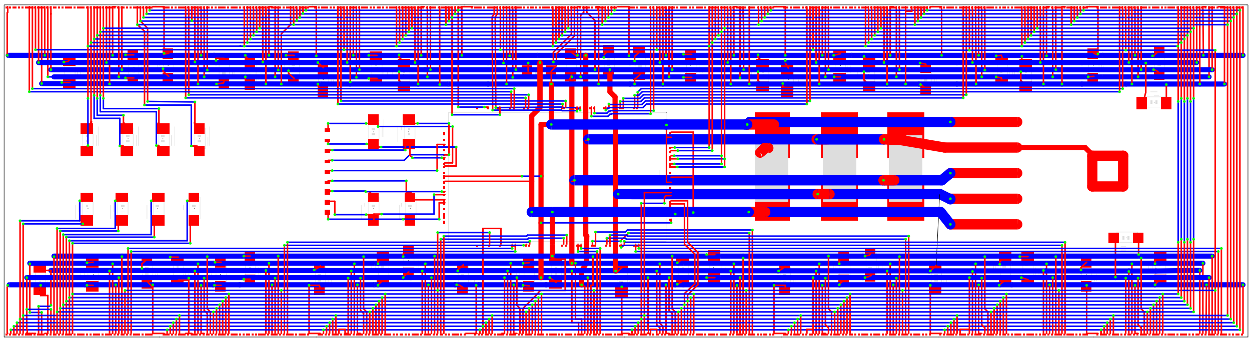

Fig. 15. Layout of both sides of the complete prototype Flex Hybrid.

parallel to each other on the same metal layer. Typical signal traces are 75 μm wide with 75 μm spaces between them. The Flex Hybrid also has passive components mounted directly on it including 12 termination resistors and 51 decoupling capacitors, although the number of decoupling capacitors may be reduced based on empirical testing. The present design calls for 0402 form factor SMD's (Surface Mount Device) for the discrete components, except for 3 tantalum capacitors, which are EIA size A. Figure 15 shows the layout of both sides of the complete prototype hybrid. The wire bond pads at the edge which allow connection to the FE chips have a pitch of 150 μm.

We are actively exploring options with several vendors including the one used for the flex connectors for the CLEO III project (GECRD), Dynamics Research Corporation (Wilmington, MA), and CERN. The first prototype will have Cu traces approximately 6 microns thick, with a barrier metal (e.g., Cr or Ni) and Au plating for the bond pads which is the same as that used for CLEO III. However, CERN has the capability to manufacture flex circuits with Al traces and that option will also be pursued.

5 Conclusion

Flex circuit designs have been made which provide required pixel module interconnections between front-end and module control chips and allow mounting of passive components such as decoupling capacitors and termination resistors. Material constraints favor high density, non-standard design rules which allow the routing to be done in two metal layers. Simulations indicate that the designs meet signal integrity requirements. Fabrication of a prototype Flex Hybrid during the next several months will allow full characterization of a complete pixel module during high energy beam tests.

6 Acknowledgments

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References

[1] Maxwell Spicelink, Ansoft Corporation.

[2] CLEO III Proposal CLNS94/1277 (unpublished).

[3] James C. Lyke et al., J. Microelectronic Systems Integration 1 (1993) 99.

[4] The flex circuits were tested in a class 10,000 clean room with a Signatone 261 microprobe station. The x, y, and z axes of the probe station were installed with stepping motors which were operated by Highland drivers and controlled by VME cards. A 486 PC computer running windows NT is used with National Instruments VXI and GPIB interfaces to automate the data taking.

[5] K. Neriyanuri, "ATLAS Pixel Detector High Density Interconnect Design and Testing of ASIC Analog Multiplexer", Masters Thesis, University of Oklahoma (1997).